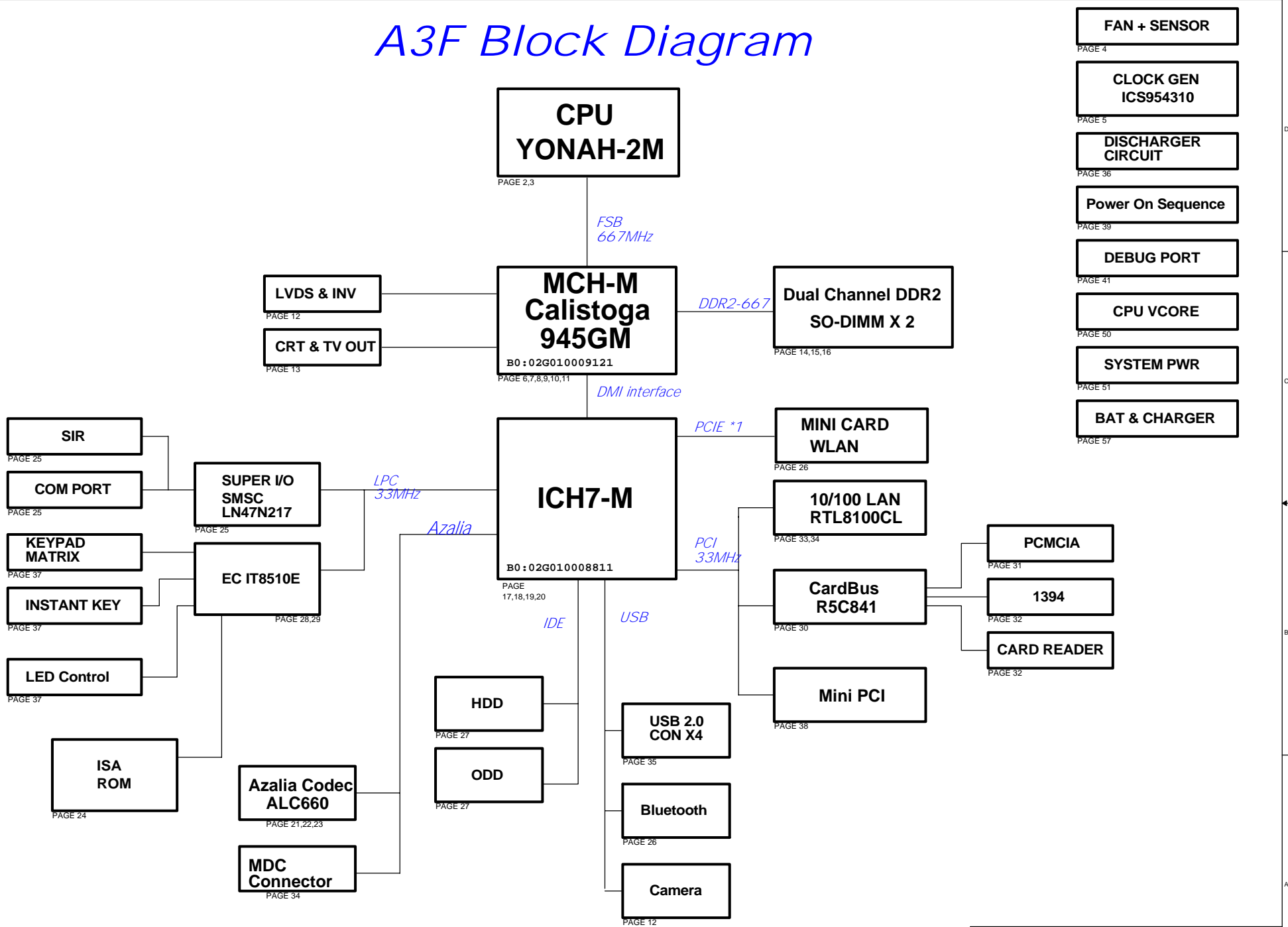
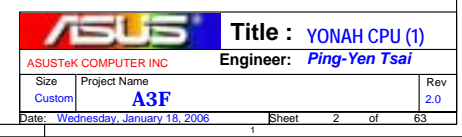
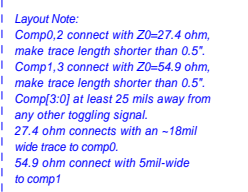


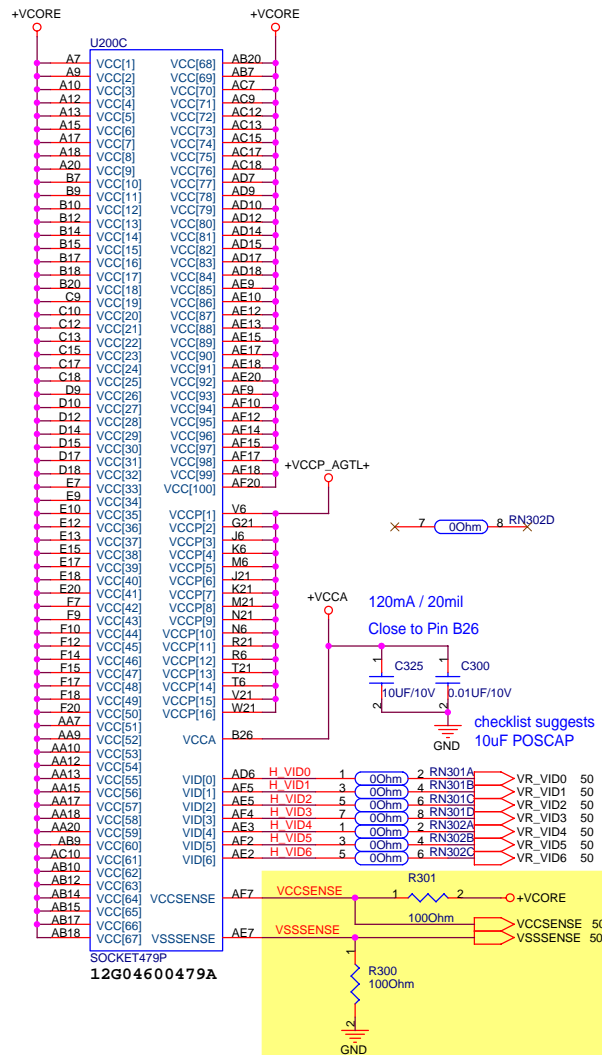
# A3F Block Diagram



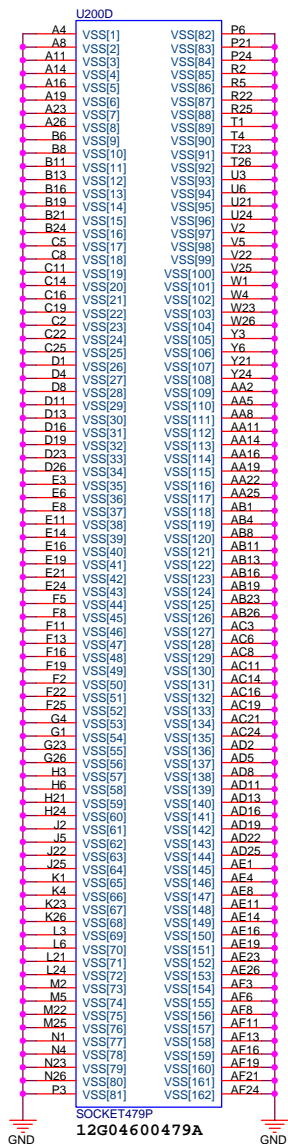


YUNAH FSB667			
LFM	TYP	HFM	
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

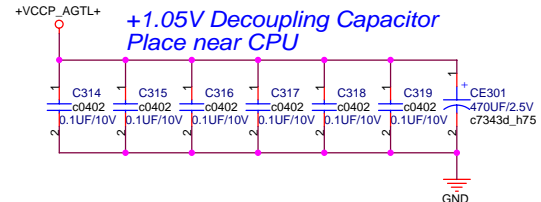
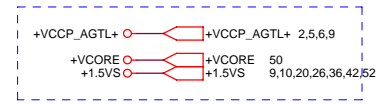
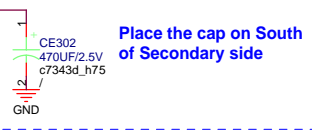
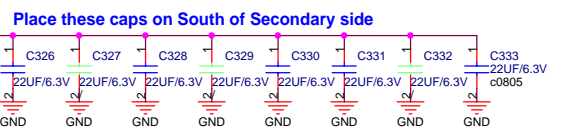
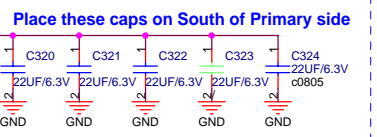
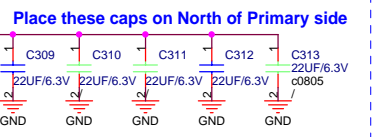
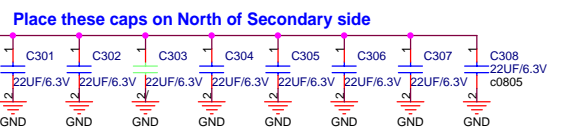
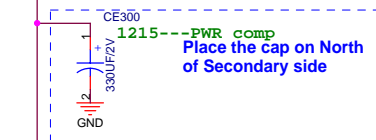
YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



**Layout Note:**  
VCCS/VSSS lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of  $Z_0 \approx 27.4 \Omega$ . The VCCS/VSSS should be length matched to within 25 mils. These resistors should be placed within 2 inch of the CPU.



+VCCORE

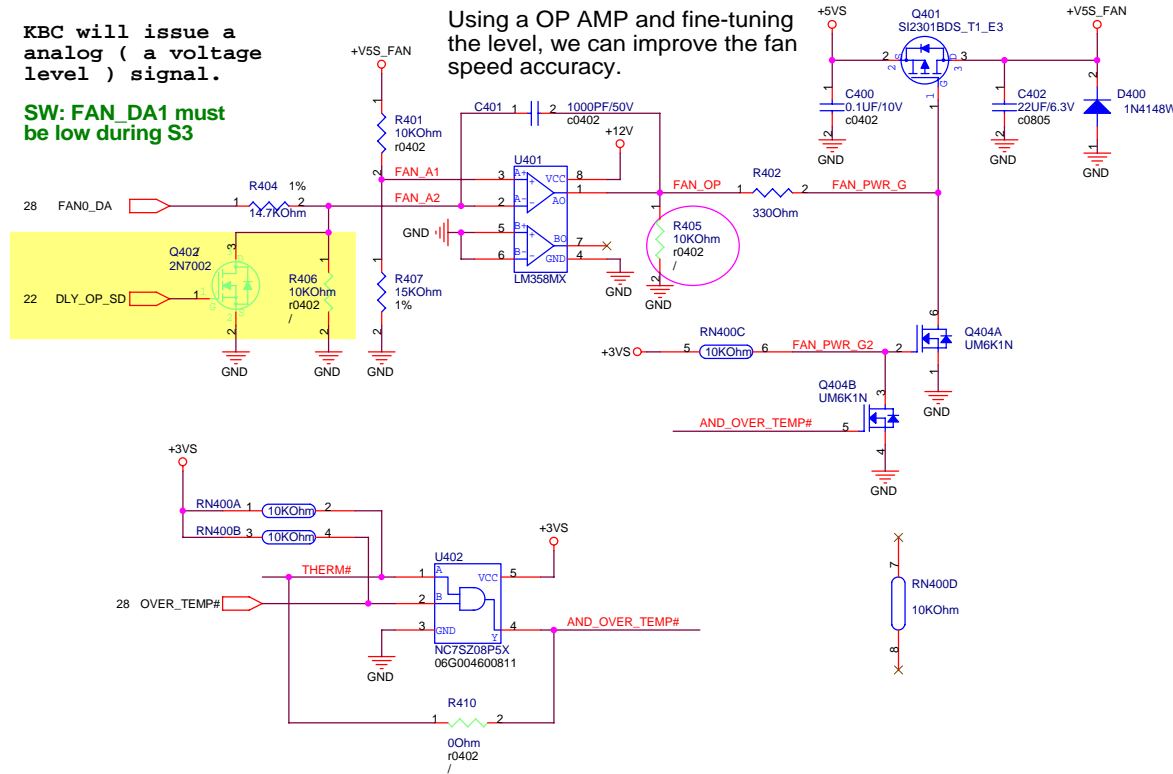


# Fan Speed Control

KBC will issue a analog ( a voltage level ) signal.

SW: FAN\_DA1 must be low during S3

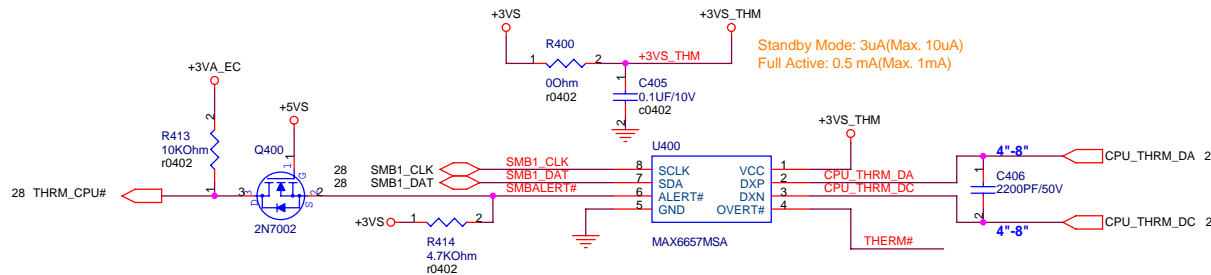
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



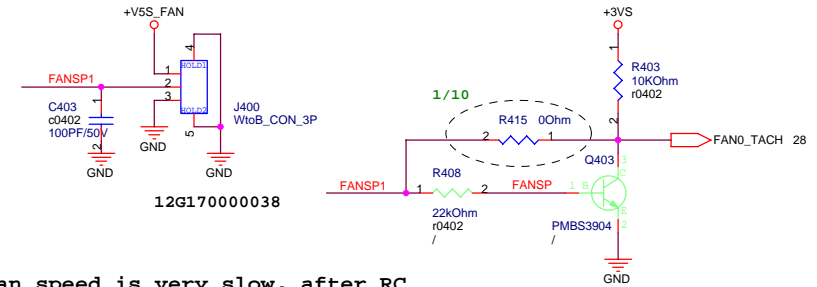
Route H\_THERMDA and H\_THERMDC on the same layer

-----OTHER SIGNALS  
12 mils  
=====GND  
10 mils  
=====H\_THERMDA(10 mils)  
10 mils  
=====H\_THERMDC(10 mils)  
10 mils  
=====GND  
12 mils  
-----OTHER SIGNALS

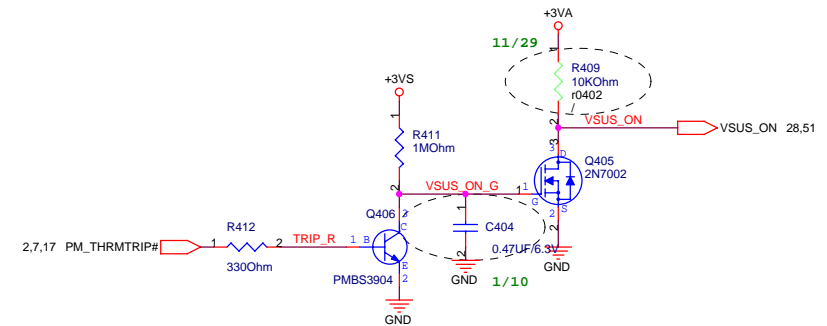
Avoid BPSB,Power



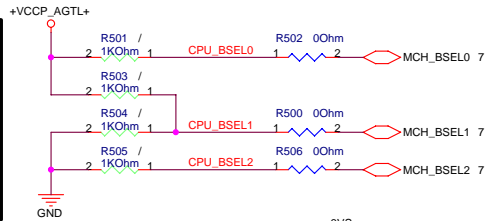
## CPU FAN



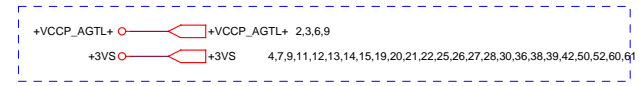
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



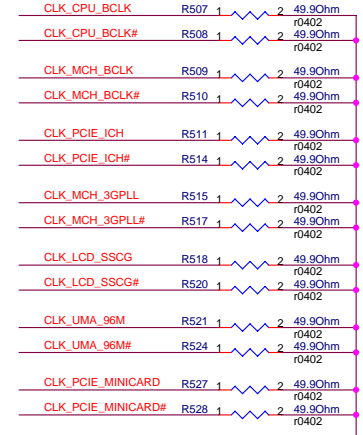
Request	Control net	Net name
PCIE_REQ1#	PCIE0( #), PCIE6( #)	None
PCIE_REQ2#	PCIE1( #), PCIE8( #)	None
PCIE_REQ3#	PCIE2( #), PCIE4( #)	CLK_PCIE_MINICARD( #)
PCIE_REQ4#	PCIE3( #), PCIE5( #), PCIE7( #)	CLK_MCH_3GPLL( #)



Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H



Layout Note:  
Place termination close to source IC

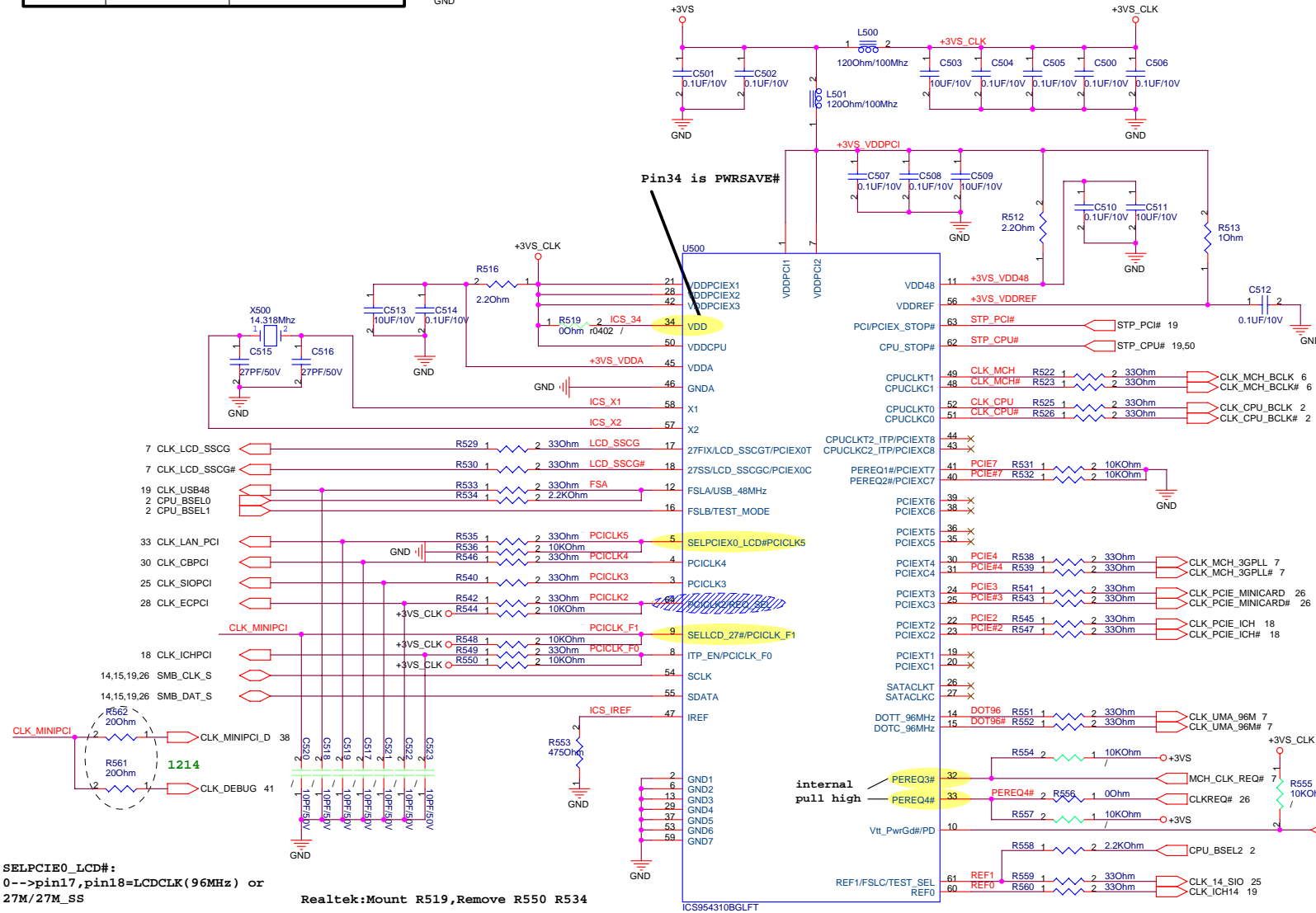


PREQ#1  
0=PCIE6 6/0 Not Controlled  
1=PCIE6 6/0 Controlled

PREQ#2  
0=PCIE8 8/1 Not Controlled  
1=PCIE8 8/1 Controlled

PREQ#3  
0=PCIE4 4/2 Not Controlled  
1=PCIE4 4/2 Controlled

PREQ#4  
0=PCIE7 7/5/3 Not Controlled  
1=PCIE7 7/5/3 Controlled



SELPICIE0\_LCD#:  
0-->pin17, pin18=LCDCLK(96MHz) or  
27M/27M\_SS

Realtek: Mount R519, Remove R550 R534

SELLCD\_27#/PCICLK\_F1:  
1-->pin17, pin18=LCDCLK(96MHz)

PCICLK2/REQ\_SEL:  
1-->pin40, pin41=PREQ1#, PREQ2#

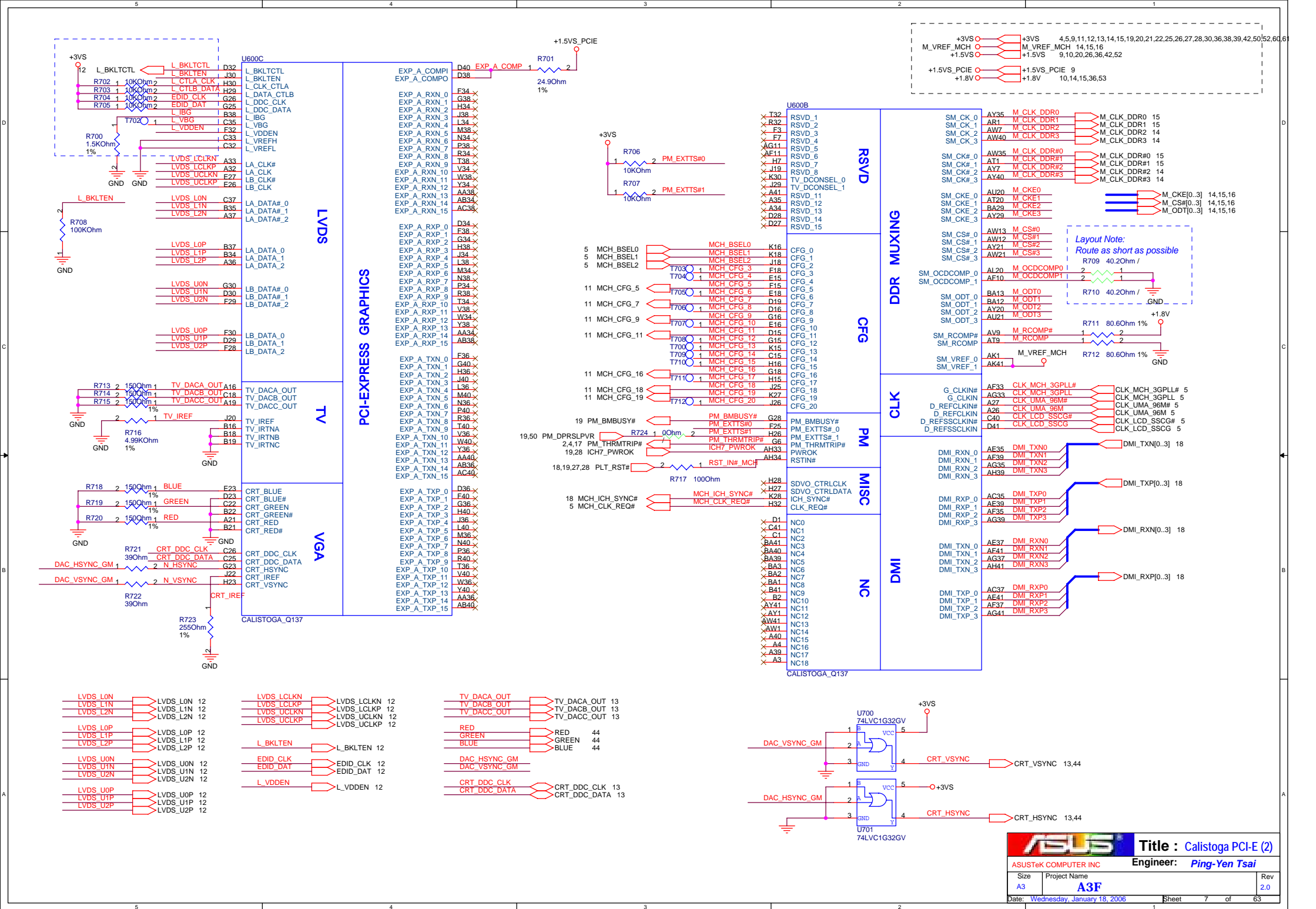
ITP\_EN/PCICLK\_F0:  
1-->CPU\_ITP pair

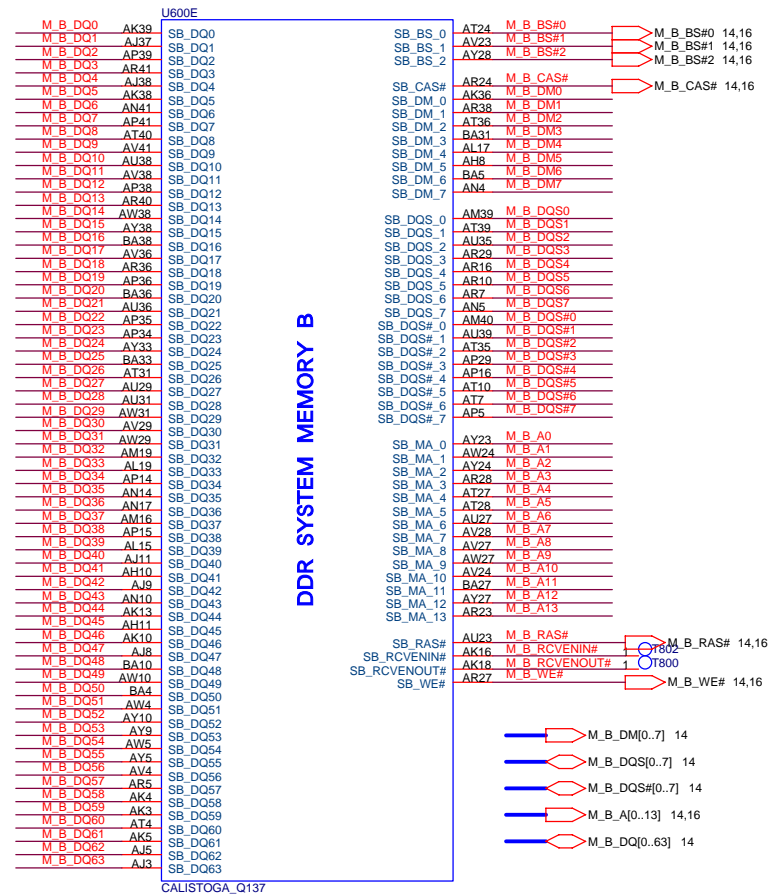
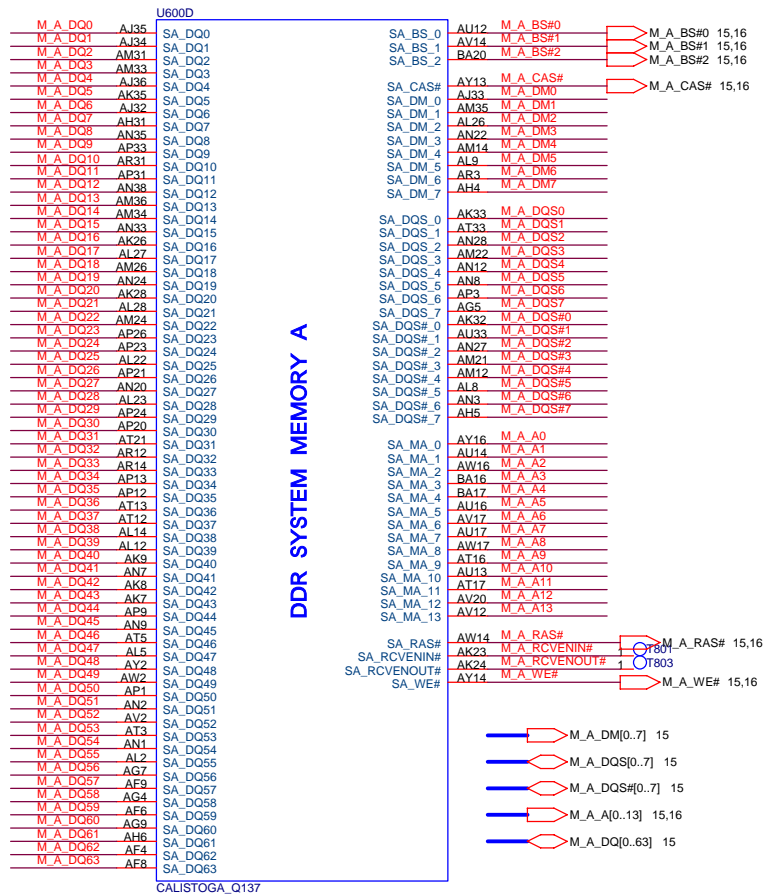
Internal Pull-Up Resistor

Internal Pull-Up Resistor

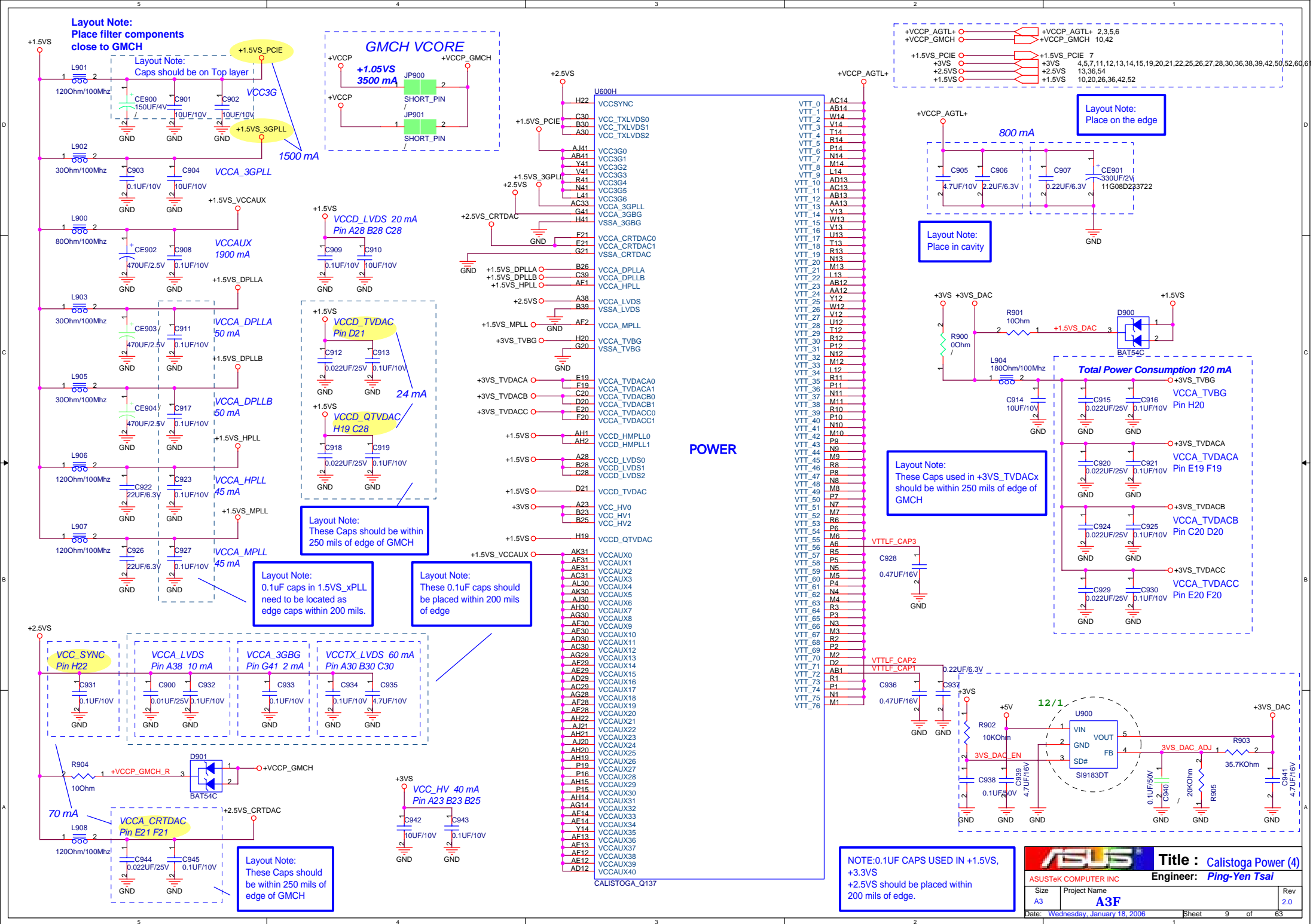


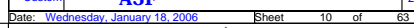


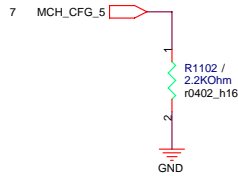




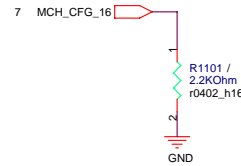




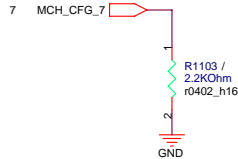




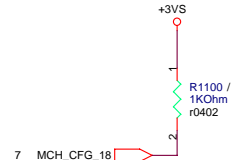
**CFG5 : DMI X2 Select**  
 LOW = DMI X 2  
**HIGH = DMI X 4 (Default)**



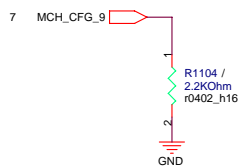
**CFG16 : FSB DYNAMIC ODT**  
 LOW = Dynamic ODT Disabled  
**HIGH = Dynamic ODT Enabled (Default)**



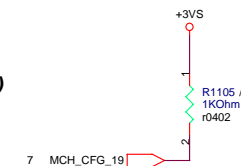
**CFG7 : CPU STRAP**  
 LOW = Reserved  
**HIGH = Mobility CPU (Default)**



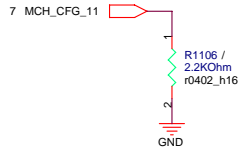
**CFG18 : GMCH Core Voltage Level**  
 LOW = 1.05V  
**HIGH = 1.5V (default)**



**CFG9 : PCIE GRAPHIC LANE**  
 LOW = REVERSE LANES  
**HIGH = NORMAL OPERATION (Default)**



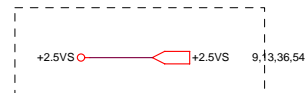
**CFG19 : DMI LANE REVERSAL**  
**LOW = NORMAL**  
 HIGH = LANES REVERSED



**CFG11 : Reserved but need to be pull low**

CFG[17..3] have internal pullup resistors.  
 CFG[19..18] have internal pulldown resistors.  
 SDVOCRTL\_DATA has internal pulldown resistors.

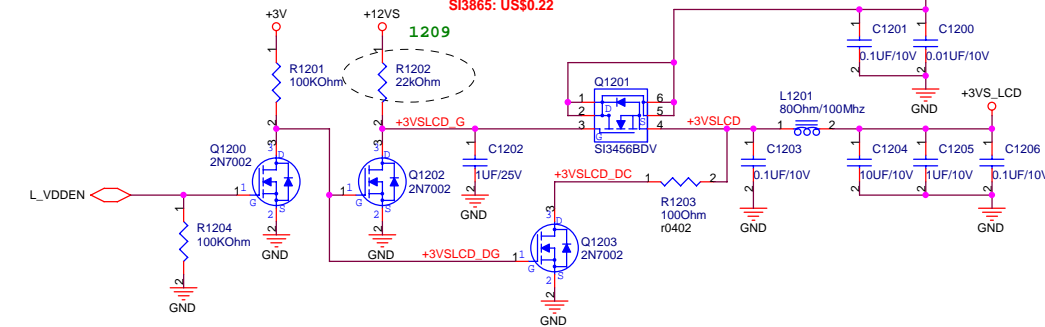
CFG All are sampled with respect to the leading edge of the GMCH PWROK		
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_C TRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



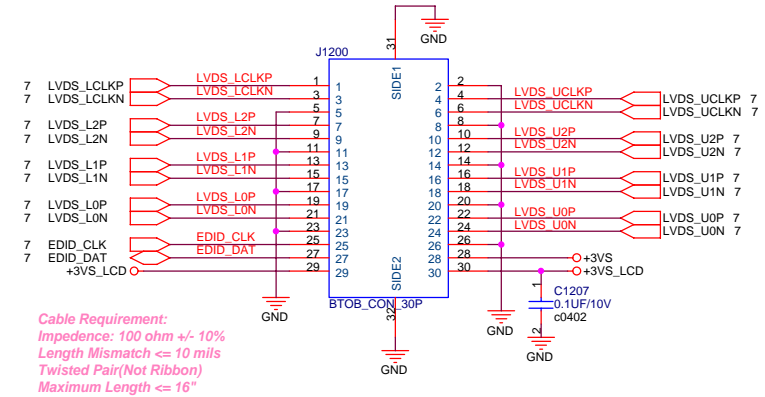
## LCD Panel Power

3~3.6V  
Full Active: 410 mA(Max. 500 mA)  
3~3.6V  
S0-S1 M: 410 mA(Max. 500 mA)

SI3865: US\$0.22



## LCD LVDS Interface

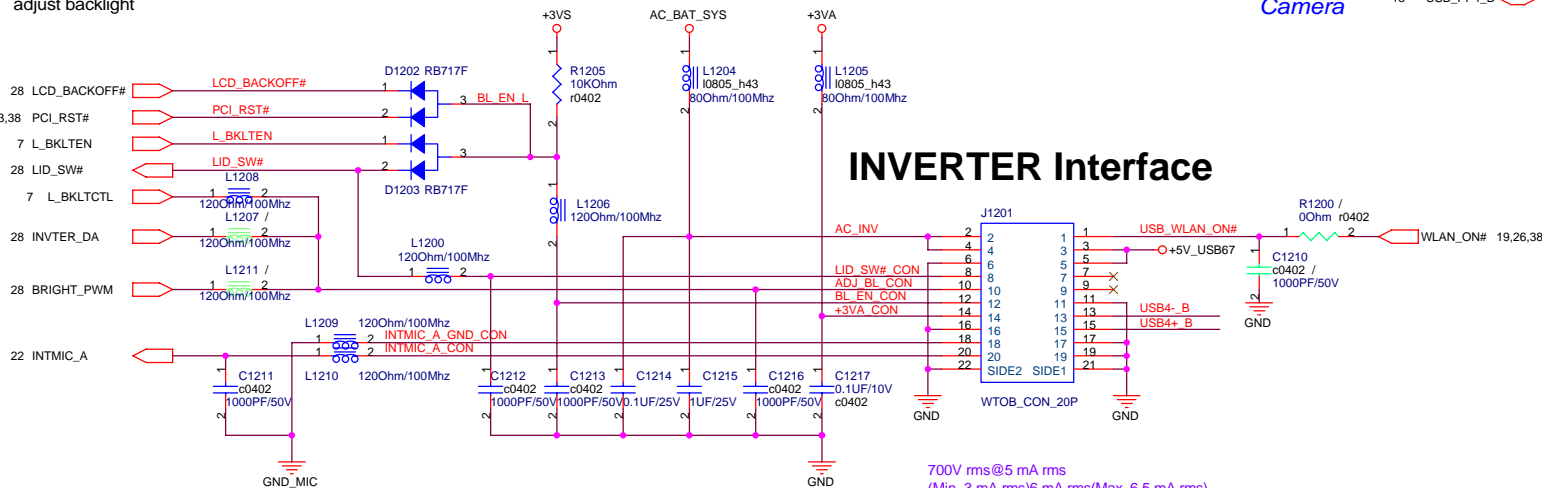


## LCD Backlight Control

BIOS  
LCD\_BACKOFF#  
When user push "Fn+F7" button  
BIOS active this pin to turn On/Off backlight

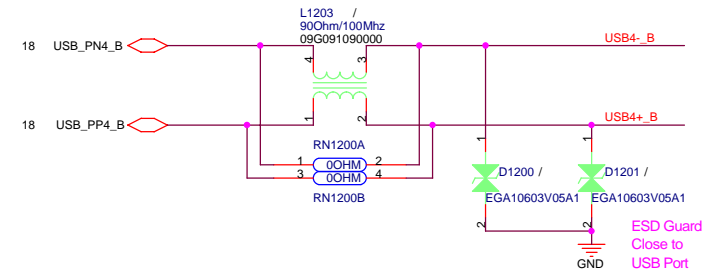
EC  
INVTER\_DA:  
EC output D/A signal ( adjust voltage level) to  
adjust backlight

*Inverter Board  
built in 14.1W  
LCD Panel*



700V rms@5 mA rms  
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

**USB4  
For  
CMOS  
Camera**

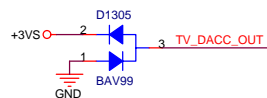
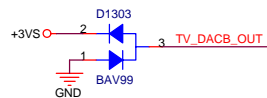
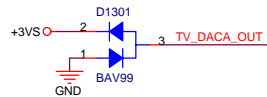
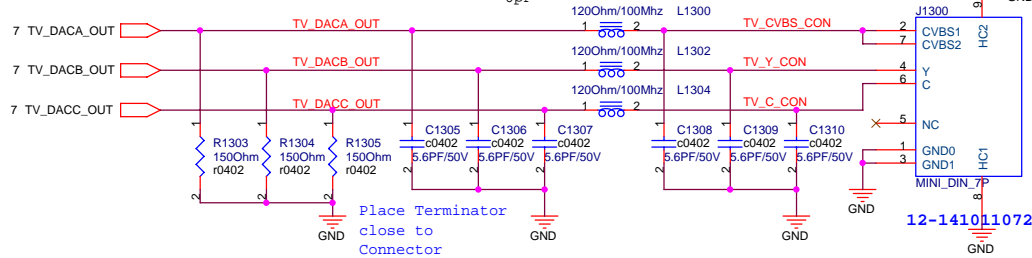


## INVERTER Interface

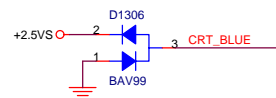
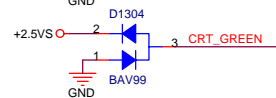
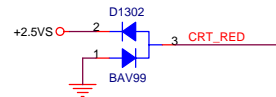
# TV OUT

12G14101107D

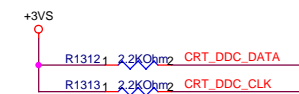
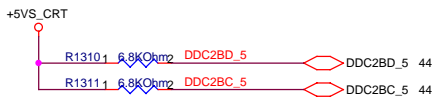
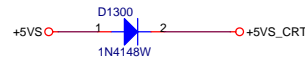
checklist suggests  
150ohm/100MHz &  
6pF



PLACE ESD Diodes near TV port

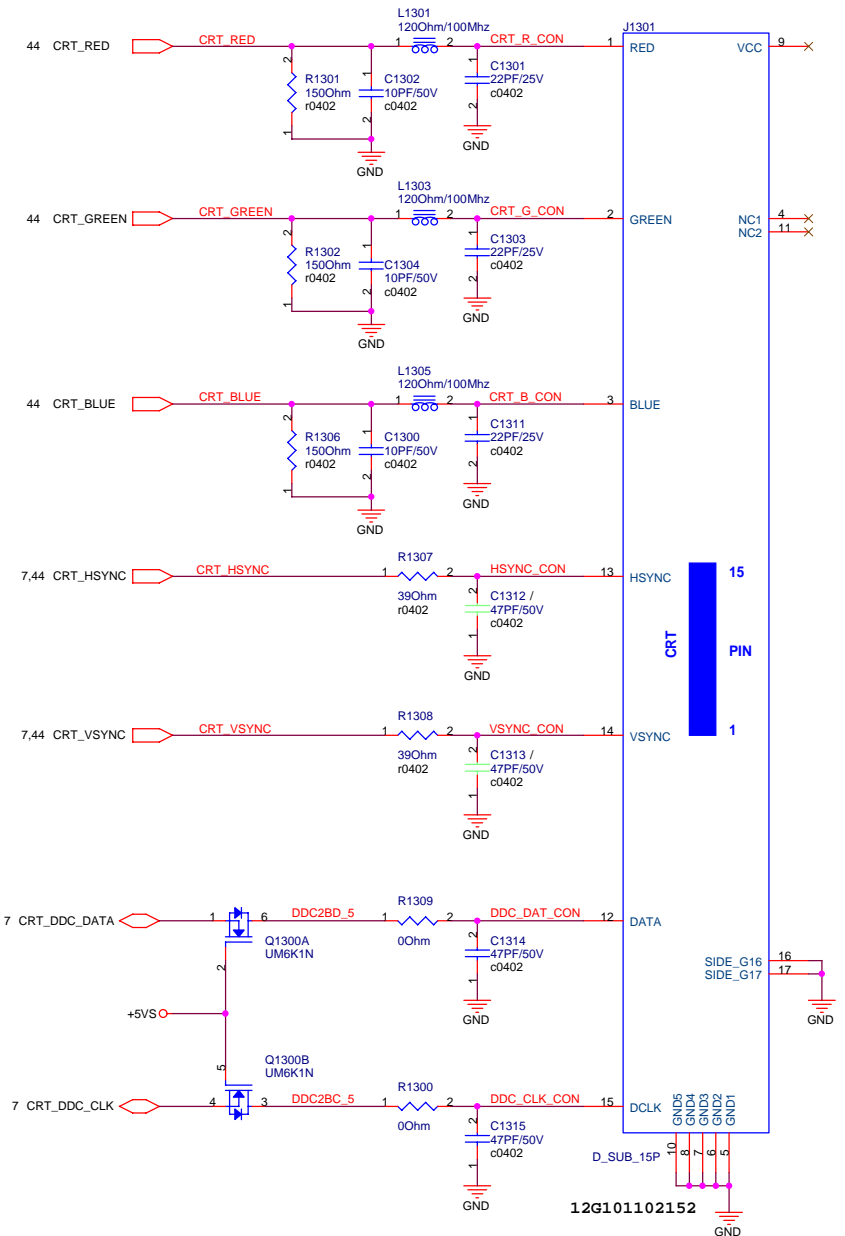


PLACE ESD Diodes near VGA port



# CRT OUT

checklist suggests 47ohm/100MHz





8 M\_B\_DQ[0..63]

8,16 M\_B\_A[0..13]

M\_B A0 102  
M\_B A1 101  
M\_B A2 100  
M\_B A3 99  
M\_B A4 98  
M\_B A5 97  
M\_B A6 94  
M\_B A7 92  
M\_B A8 93  
M\_B A9 91  
M\_B A10 105  
M\_B A11 90  
M\_B A12 89  
M\_B A13 116  
86  
84  
85

U1400A

DQ0 5  
DQ1 7  
DQ2 17  
DQ3 19  
DQ4 4  
DQ5 6  
DQ6 14  
DQ7 16  
DQ8 23  
DQ9 25  
DQ10 35  
DQ11 37  
DQ12 20  
DQ13 22  
DQ14 36  
DQ15 38  
DQ16 43  
DQ17 45  
DQ18 55  
DQ19 57  
DQ20 44  
DQ21 46  
DQ22 56  
DQ23 58  
DQ24 61  
DQ25 63  
DQ26 73  
DQ27 75  
DQ28 62  
DQ29 64  
DQ30 74  
DQ31 76

M\_B DQ1 5  
M\_B DQ5 7  
M\_B DQ2 17  
M\_B DQ3 19  
M\_B DQ4 4  
M\_B DQ6 14  
M\_B DQ7 16  
M\_B DQ8 23  
M\_B DQ12 25  
M\_B DQ9 35  
M\_B DQ11 37  
M\_B DQ13 20  
M\_B DQ10 22  
M\_B DQ14 36  
M\_B DQ15 38  
M\_B DQ20 43  
M\_B DQ17 45  
M\_B DQ23 55  
M\_B DQ22 57  
M\_B DQ21 44  
M\_B DQ16 46  
M\_B DQ19 56  
M\_B DQ18 58  
M\_B DQ29 61  
M\_B DQ28 63  
M\_B DQ27 73  
M\_B DQ30 74  
M\_B DQ31 76

8,16 M\_B\_BS#2

M\_B\_BS#2

8,16 M\_B\_BS#0

M\_B\_BS#0

8,16 M\_B\_BS#1

M\_B\_BS#1

7,16 M\_CS#2

M\_CS#2

7,16 M\_CS#3

M\_CS#3

7 M\_CLK\_DDR3

M\_CLK\_DDR3

7 M\_CLK\_DDR#3

M\_CLK\_DDR#3

7 M\_CLK\_DDR2

M\_CLK\_DDR2

7 M\_CLK\_DDR#2

M\_CLK\_DDR#2

7,16 M\_CKE2

M\_CKE2

7,16 M\_CKE3

M\_CKE3

8,16 M\_B\_CAS#

M\_B\_CAS#

8,16 M\_B\_RAS#

M\_B\_RAS#

8,16 M\_B\_WE#

M\_B\_WE#

11/14  
+3VS  
R1401 2 r0402  
10KOhm

5,15,19,26 SMB\_CLK\_S  
5,15,19,26 SMB\_DAT\_S

SMB\_CLK\_S

SMB\_DAT\_S

7,16 M\_ODT2

M\_ODT2

7,16 M\_ODT3

M\_ODT3

For Data Swap

DM0 10

DM1 26

DM2 52

DM3 67

DM4 130

DM5 147

DM6 170

DM7 185

M\_B DQS0 13

M\_B DQS1 31

M\_B DQS2 51

M\_B DQS3 70

M\_B DQS4 131

M\_B DQS5 148

M\_B DQS6 169

M\_B DQS7 188

M\_B DQS#0 11

M\_B DQS#1 29

M\_B DQS#2 49

M\_B DQS#3 68

M\_B DQS#4 129

M\_B DQS#5 146

M\_B DQS#6 167

M\_B DQS#7 186

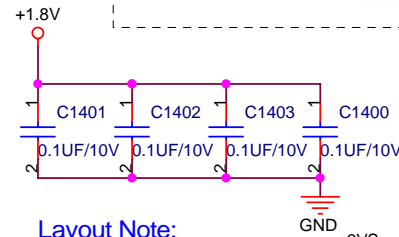
DDR\_DIMM\_200P\_A  
12G025122007

8 M\_B\_DM[0..7]

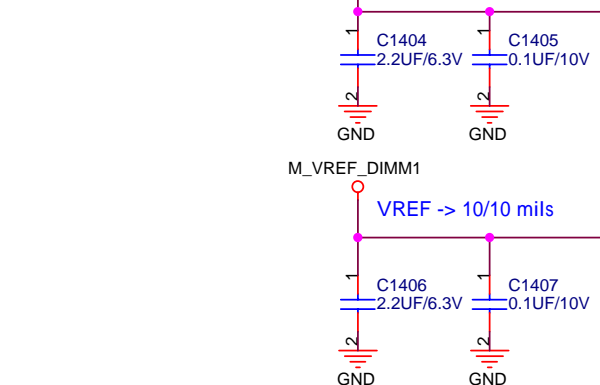
8 M\_B\_DQS[0..7]

8 M\_B\_DQS#[0..7]

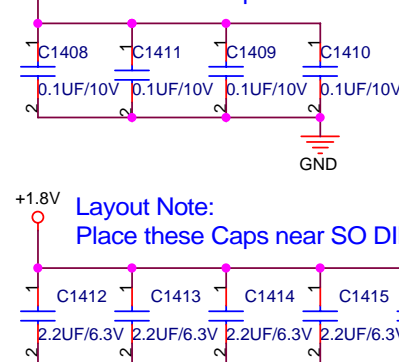
M\_VREF\_DIMM1 7,15,16  
+1.8V 7,10,15,36,53  
+3VS 4,5,7,9,11,12,13,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61



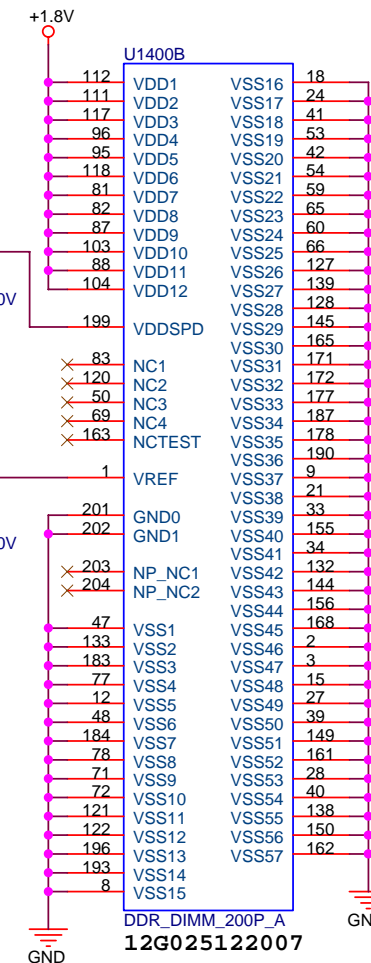
Layout Note:  
Place these resistors  
near the GMCH



Layout Note:  
Place these Caps near SO DIMM 1



Layout Note:  
Place these Caps near SO DIMM 1



Title : DDR2\_SO-DIMM(1)

ASUSTeK COMPUTER INC

Engineer: Ping-Yen Tsai

Size  
A4

Project Name  
A3F

Rev  
2.0

Date: Wednesday, January 18, 2006

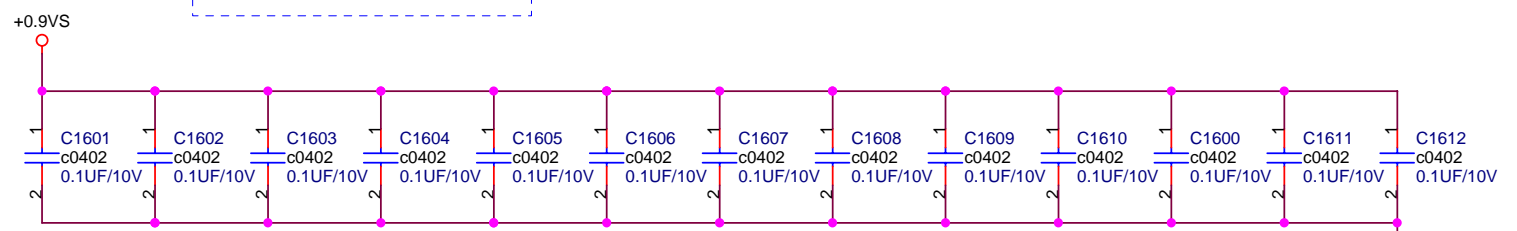
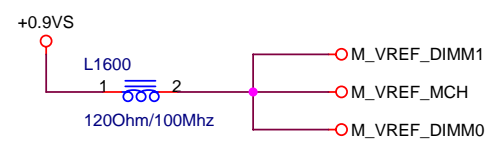
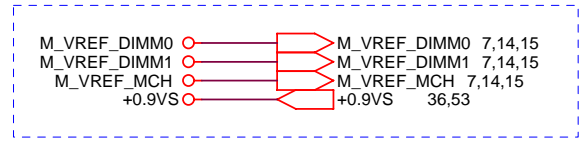
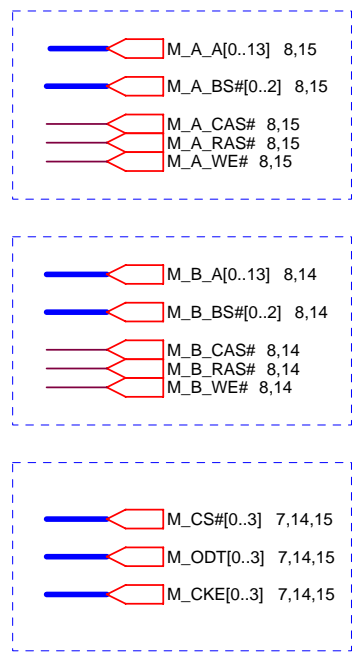
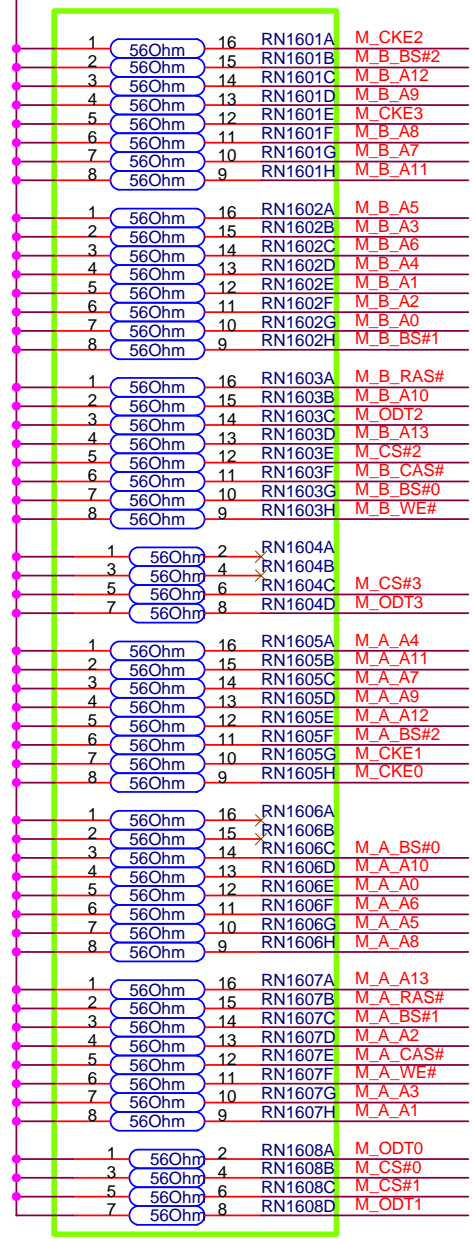
Sheet 14 of 63



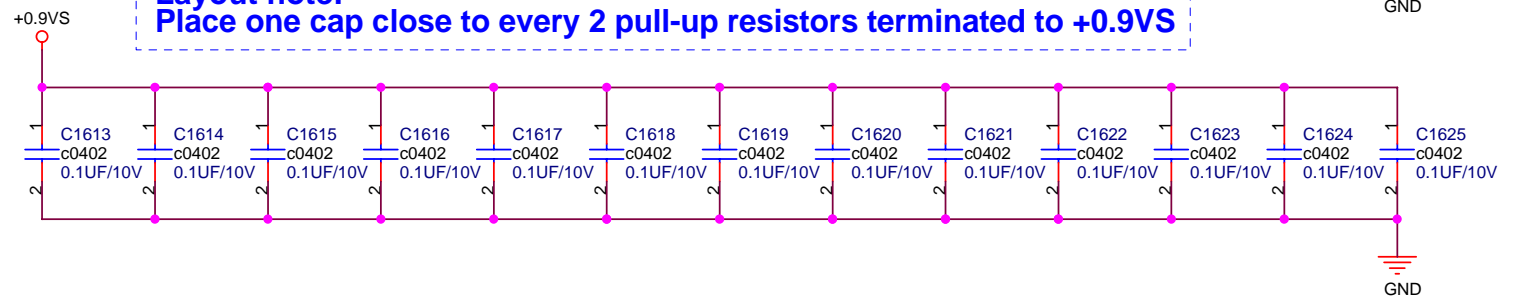


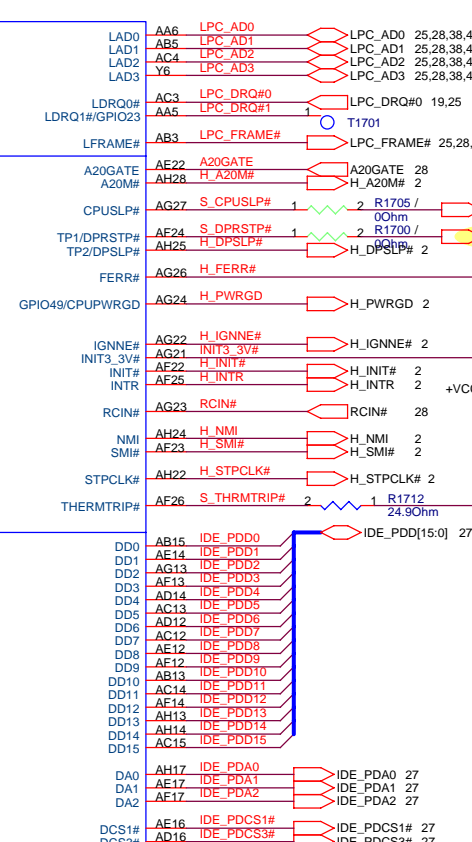
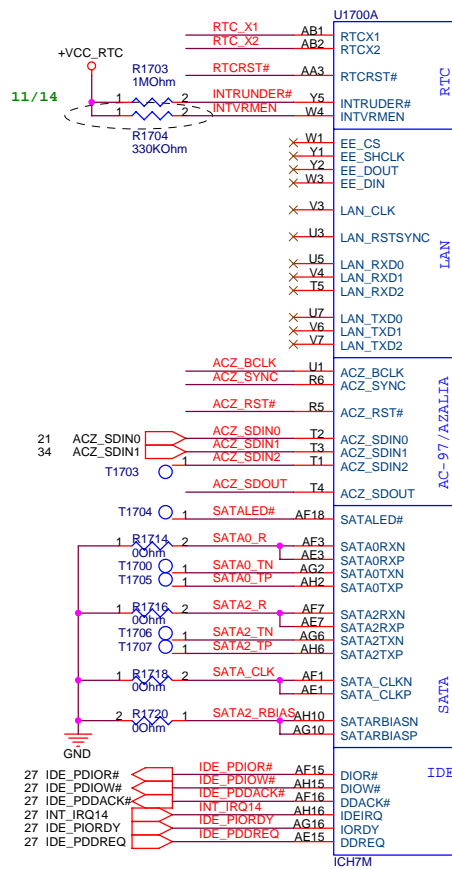
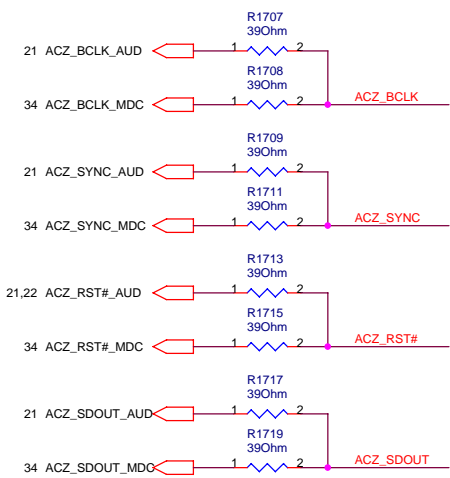
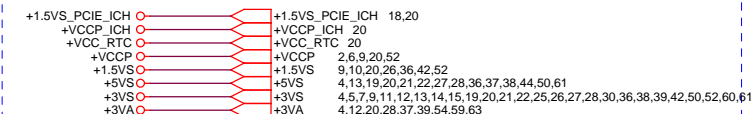
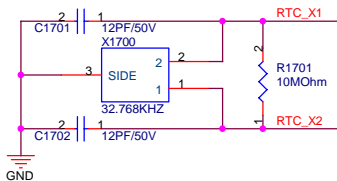
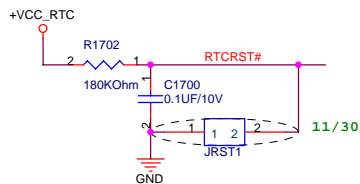
+0.9VS

NEED TO SWAP



Layout note:  
Place one cap close to every 2 pull-up resistors terminated to +0.9VS





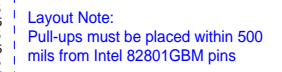
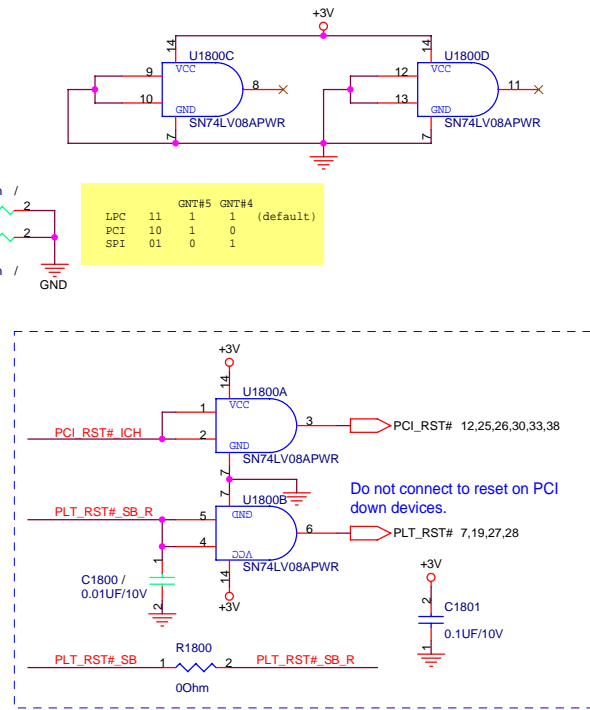
DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor

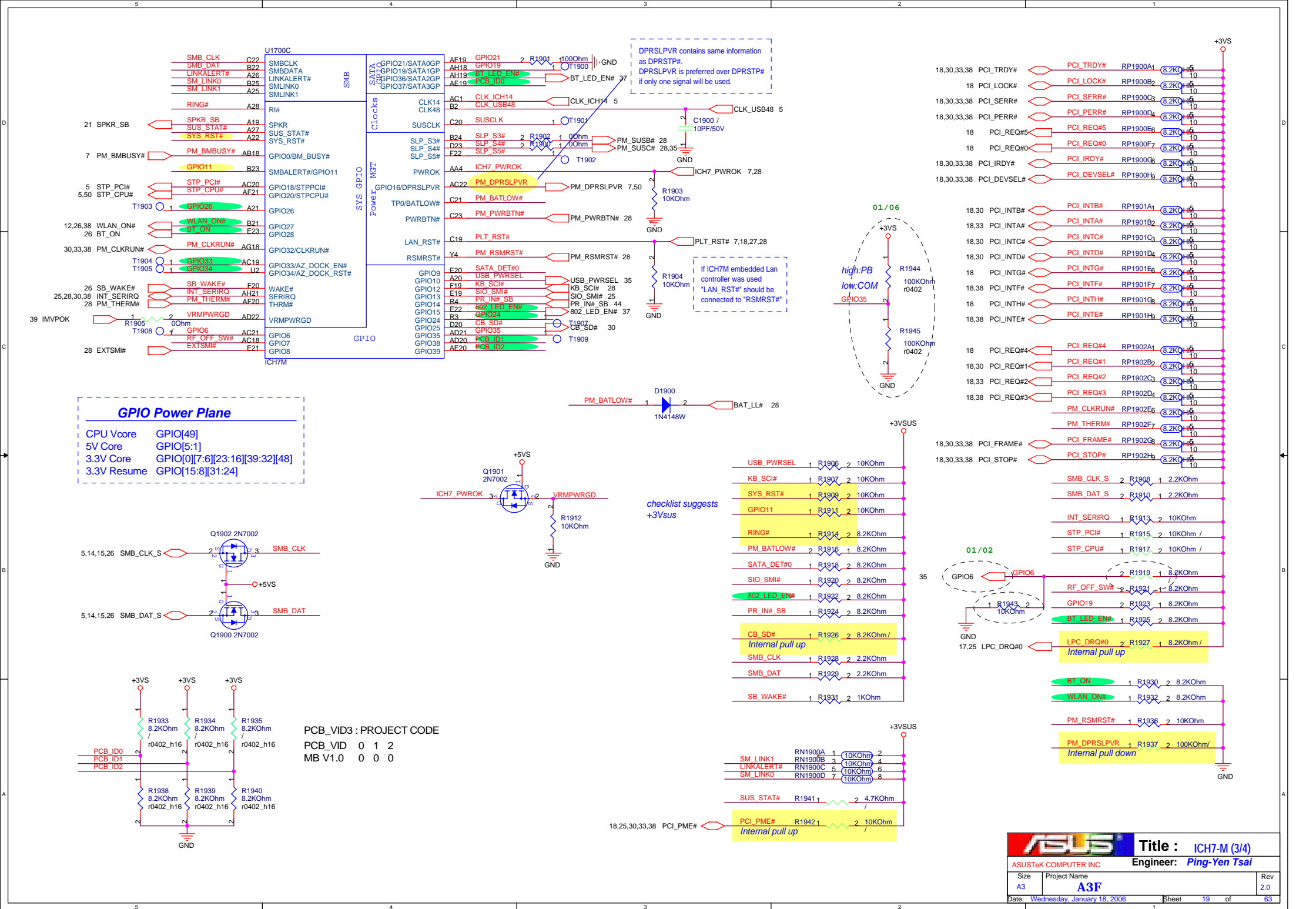
ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17#		GNT5# GNT4#	PU
GNT4#/GPIO48	PWROK rising	0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16		should not be pulled high	PD
DPRSTP#		should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSusi_05 VRM	
LINKALERT#		REQUIRE an external pull-up R	Need
REQ[4:1]#	PWROK rising		PU
SATALED#		should not be pulled low	Conditional
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

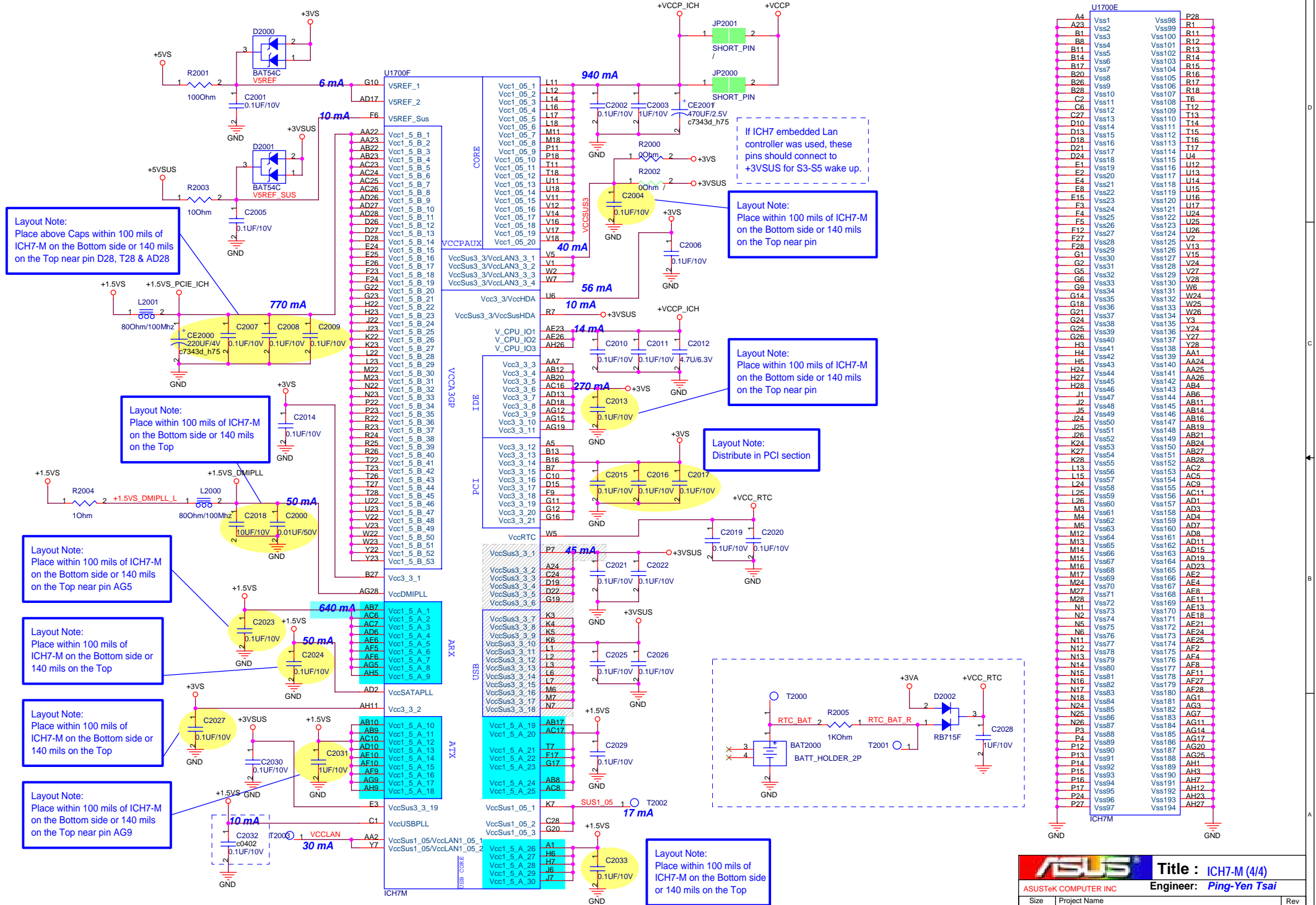
Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A
Mini-PCI	AD19	REQ3#/GNT3#	E, F



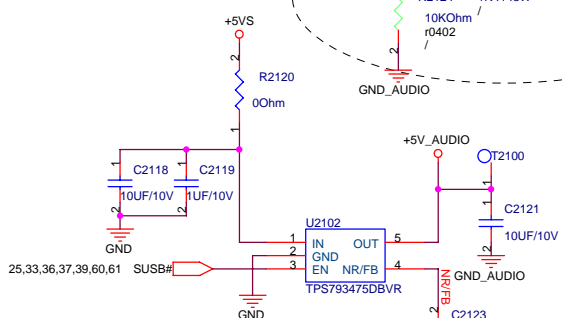
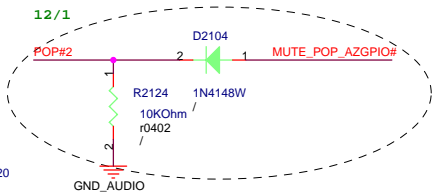
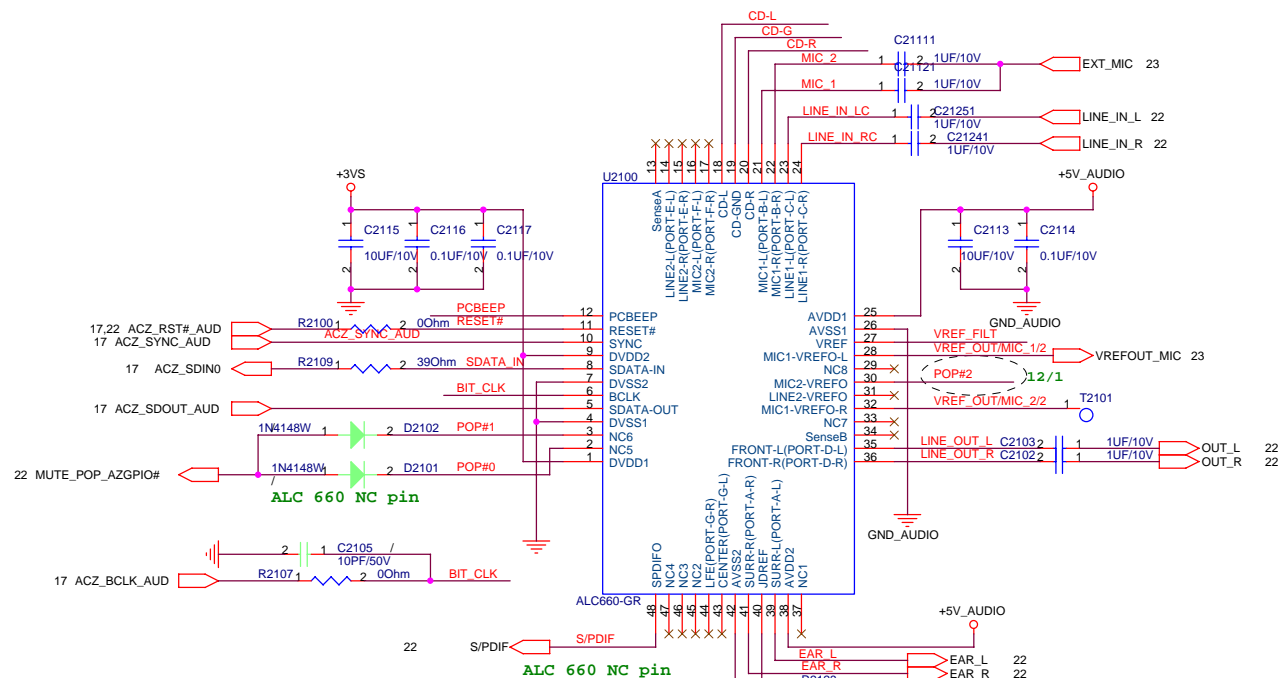
Port 0	Conn. 0
Port 1	Conn. 1
Port 2	Conn. 2
Port 3	Conn. 3
Port 4	NC
Port 5	Bluetooth
Port 6	CMOS Camera
Port 7	Mini Card



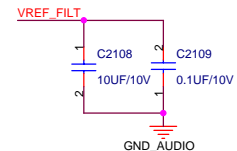
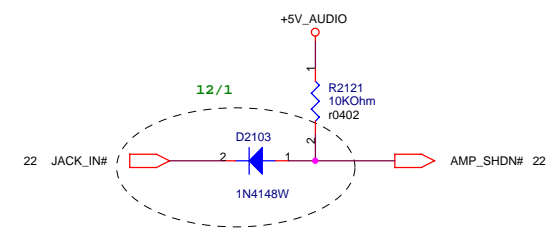
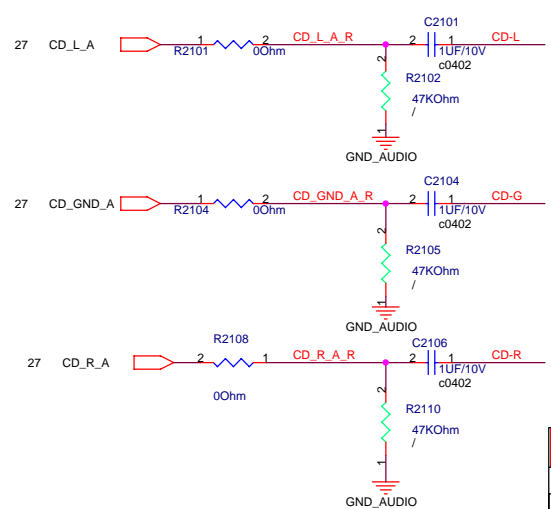
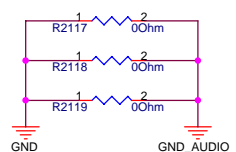
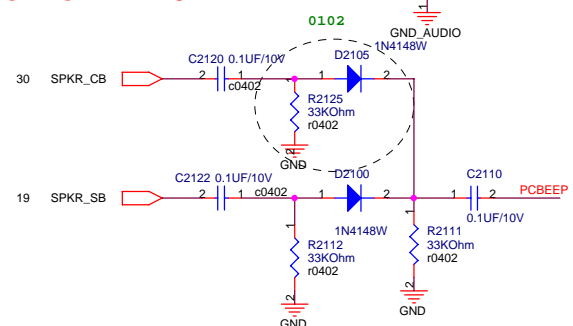


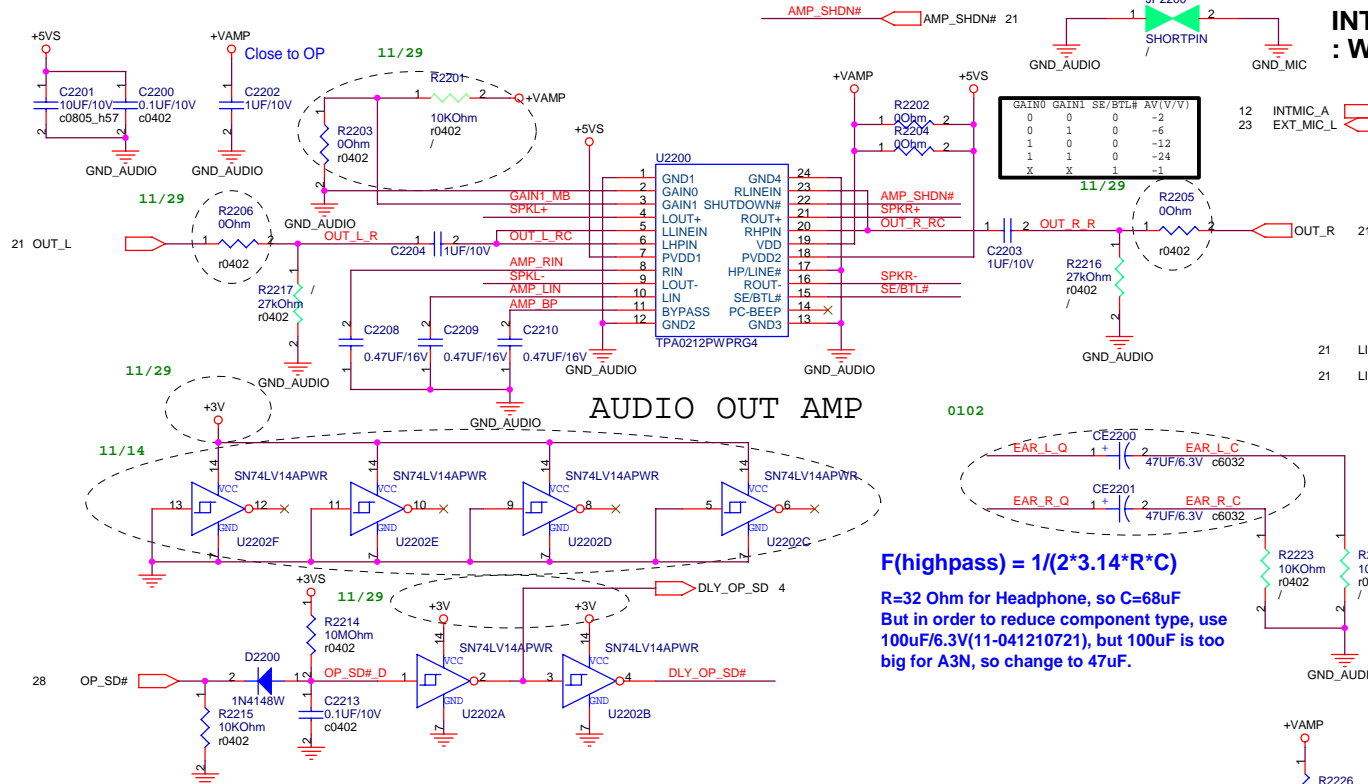






5V-5VA LDO





$F(\text{highpass}) = 1/(2 \times 3.14 \times R \times C)$   
 $R = 32 \text{ Ohm}$  for Headphone, so  $C = 68 \mu\text{F}$   
 But in order to reduce component type, use  $100 \mu\text{F}/6.3\text{V}$  (11-041210721), but  $100 \mu\text{F}$  is too big for A3N, so change to  $47 \mu\text{F}$ .

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add  $OP\_SD\#$  to control the turn-on timing.

21 MUTE\_POP\_AZGPIO#

11/29

17,21 ACZ\_RST#\_AUD

But when system resume from S3, pop noise is behind  $OP\_SD\#$  pull high. Add a delay circuit to prevent it.

INTMIC\_A:GND\_AUDIO

: W/P/X = 12/5/15mils

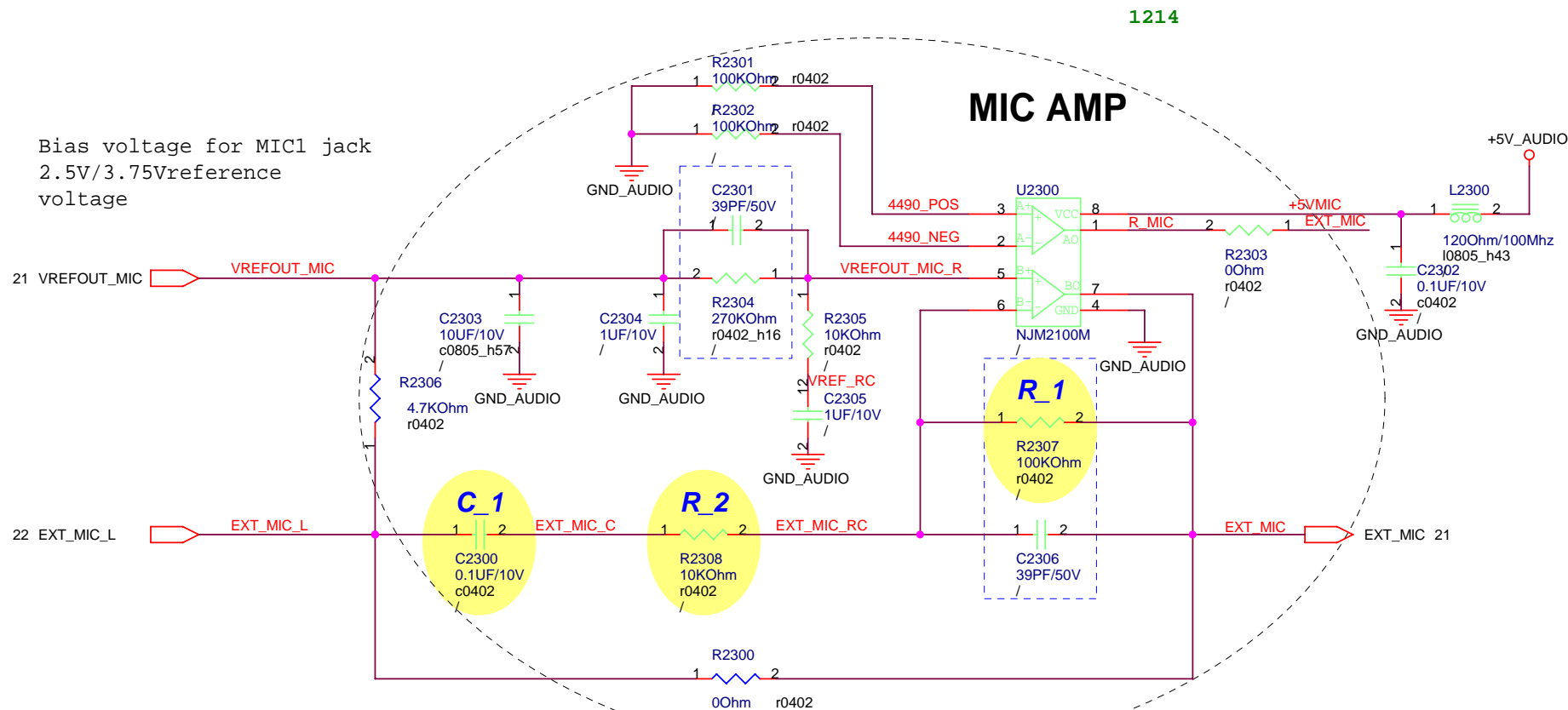
**MIC JACK**

to pre AMP

**LINE IN JACK**

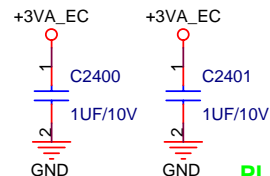
**HEADPHONE & S/PDIF**

**SPEAKER CONN.**



**High-Pass Filter Cutoff Frequency**  
 $F_c = 1 / (2 \times 3.14 \times C_1 \times R_2) = 159 \text{ Hz}$

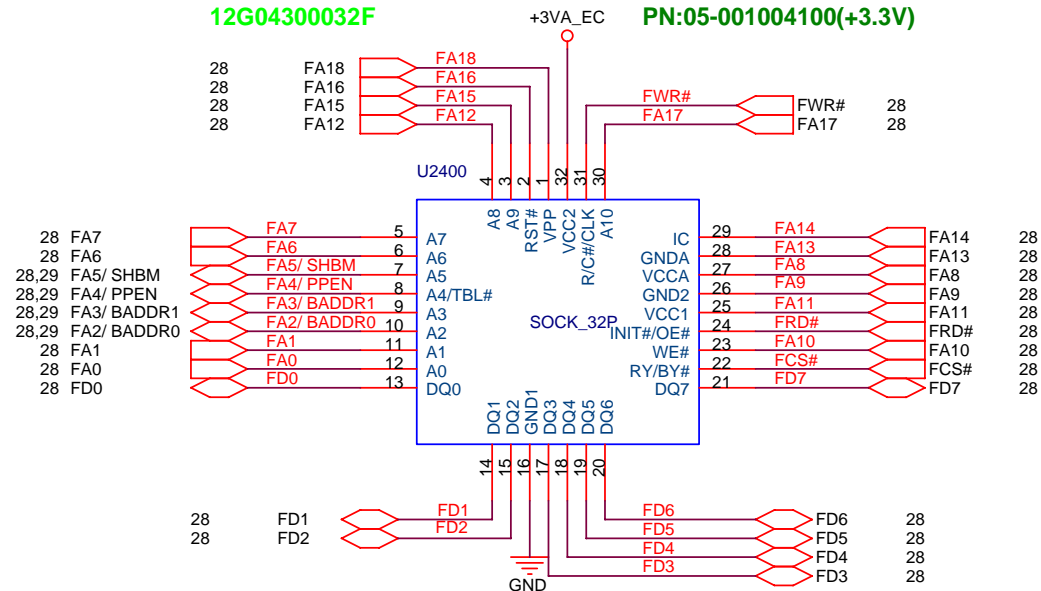
**Gain = - R\_1 / R\_2 = -10**



ISA ROM

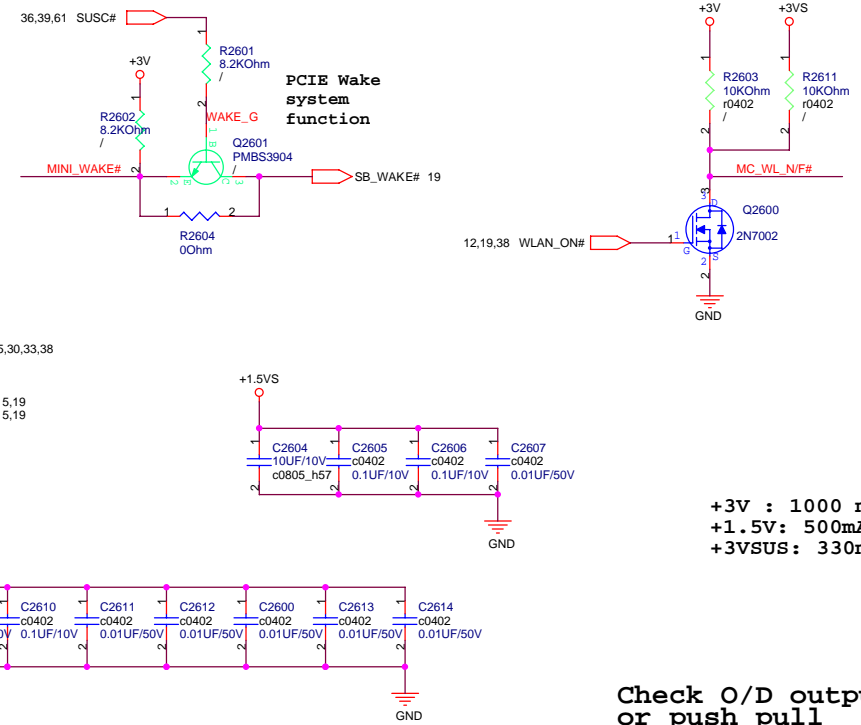
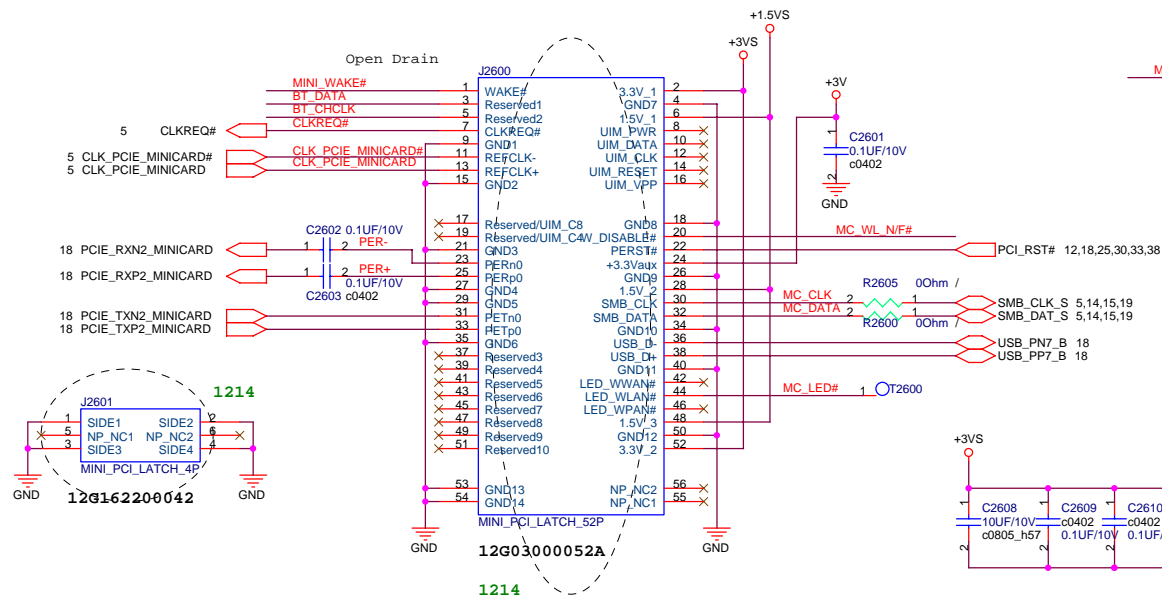
PLCC32 Socket PN:  
12G04300032F

SST-PLCC32 4Mbits Flash ROM  
PN:05-001004100(+3.3V)

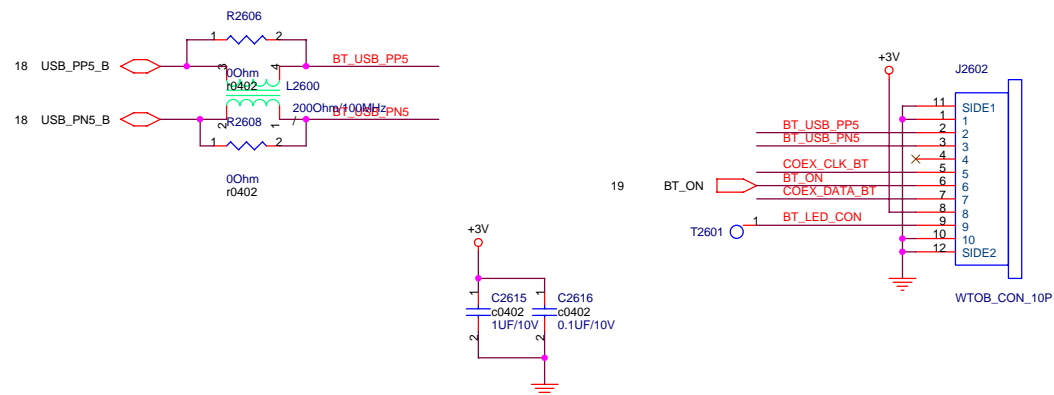




## MINI PCIEX CONNECTOR



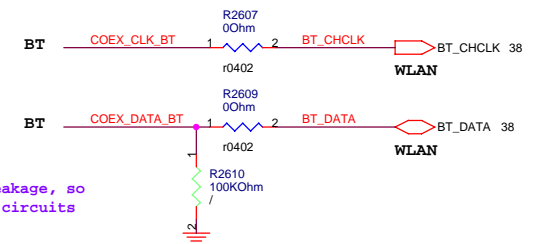
## BLUETOOTH CONNECTOR



```
Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT
```

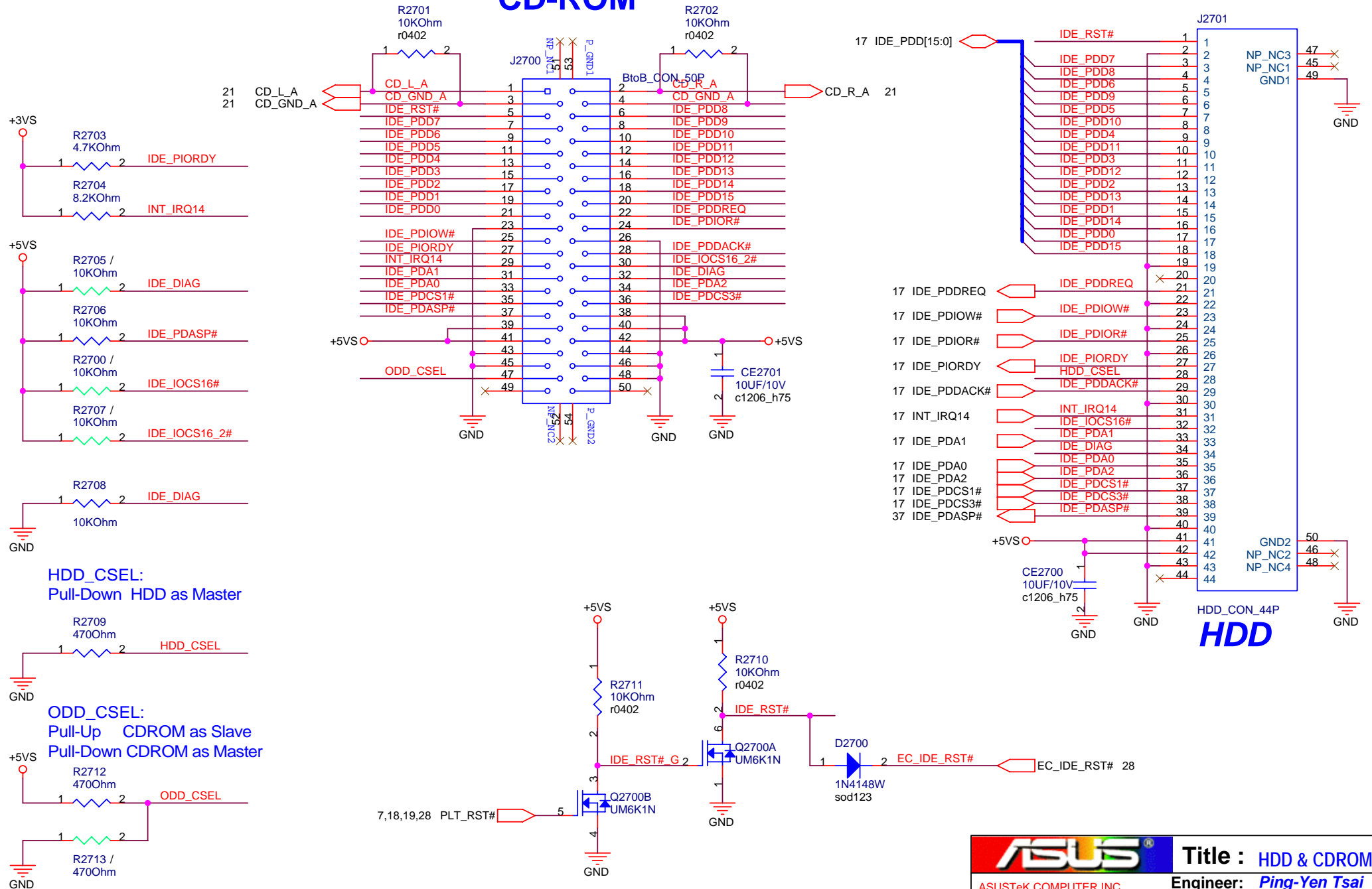
```
BT_ON 3.3V at
GPIO38
```

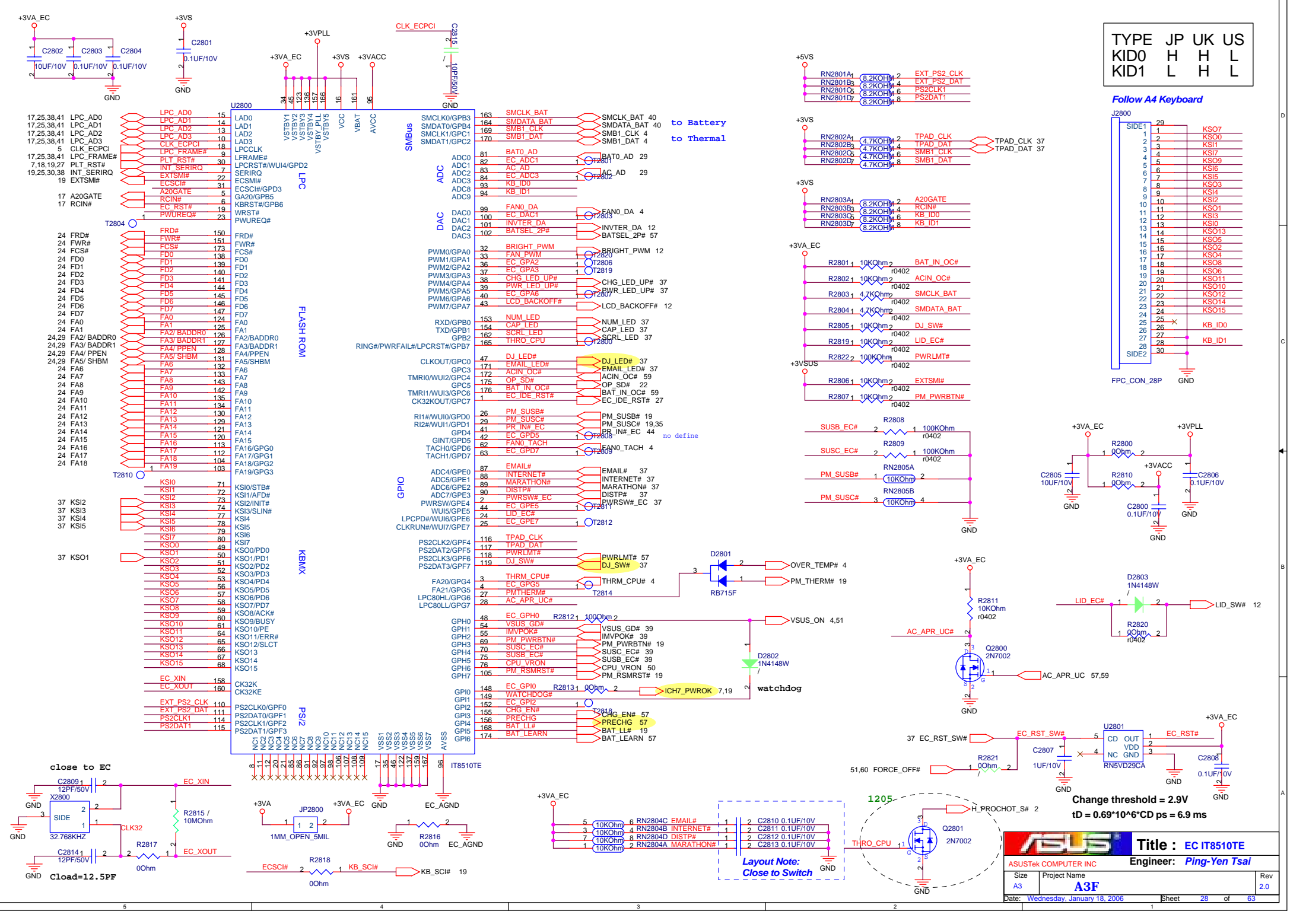
BT Module has no leakage, so  
discard PMOS block circuits





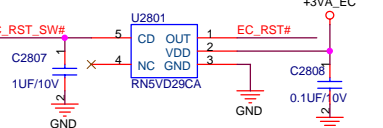
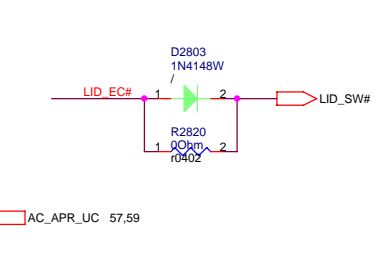
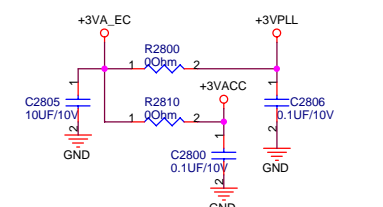
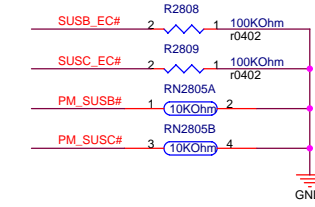
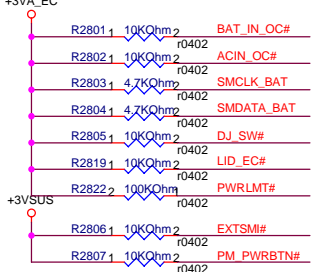
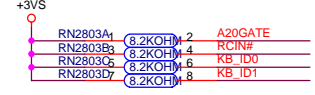
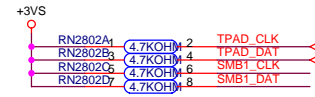
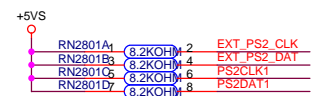
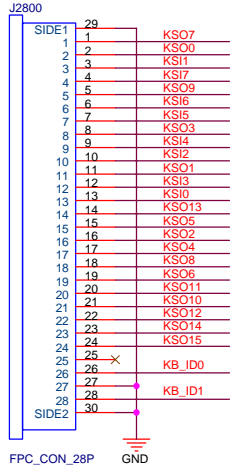
# CD-ROM





TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

Follow A4 Keyboard



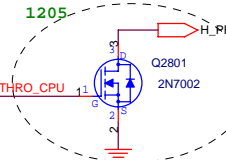
Change threshold = 2.9V  
tD = 0.69\*10^6 CD ps = 6.9 ms

**ASUS** Title : EC IT8510TE  
ASUSTek COMPUTER INC Engineer: Ping-Yen Tsai

Size	Project Name	Rev
A3	A3F	2.0

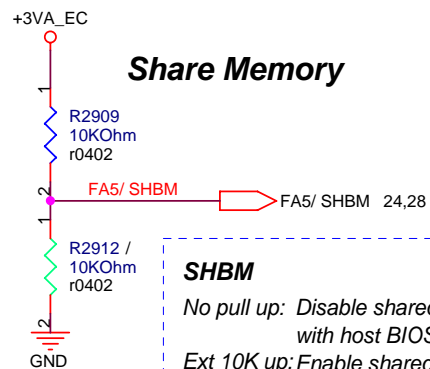
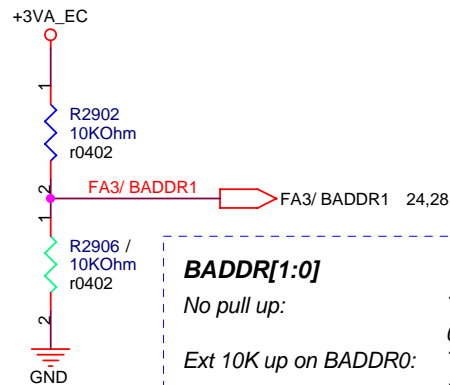
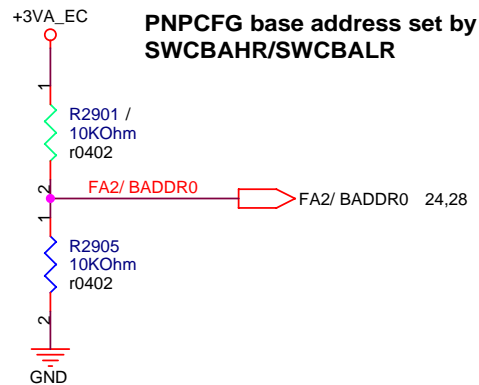
Date: Wednesday, January 18, 2006 Sheet 28 of 63

Layout Note:  
Close to Switch



## EC Hardware Strap

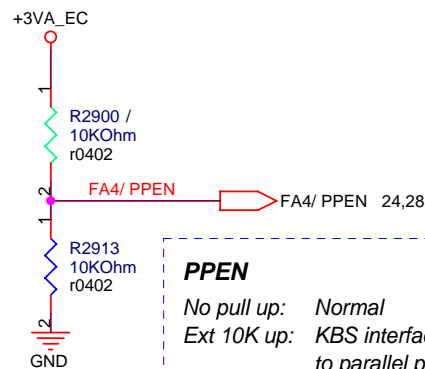
Strap value sampled after  
VSTBY power up reset



### SHBM

No pull up: Disable shared memory with host BIOS

Ext 10K up: Enable shared memory with host BIOS



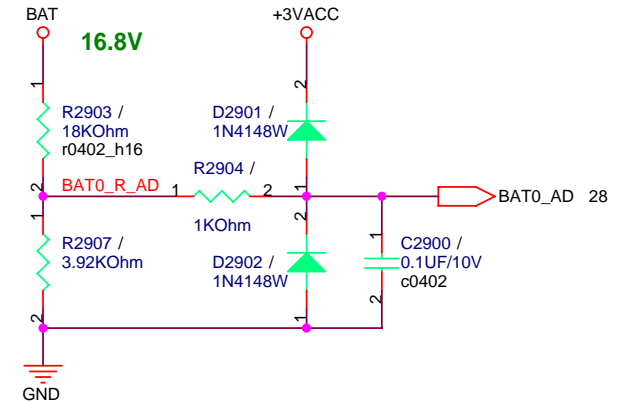
### PPEN

No pull up: Normal

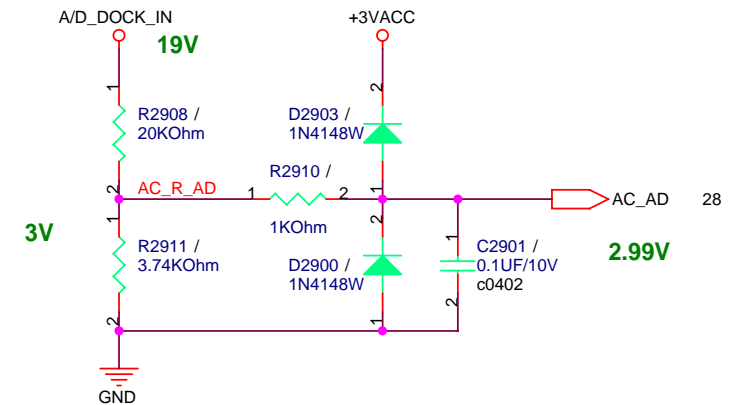
Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.

## EC ADC

### Battery



### Adaptor



Title : EC IT8510TE(2/2)

ASUSTek COMPUTER INC

Engineer: Ping-Yen Tsai

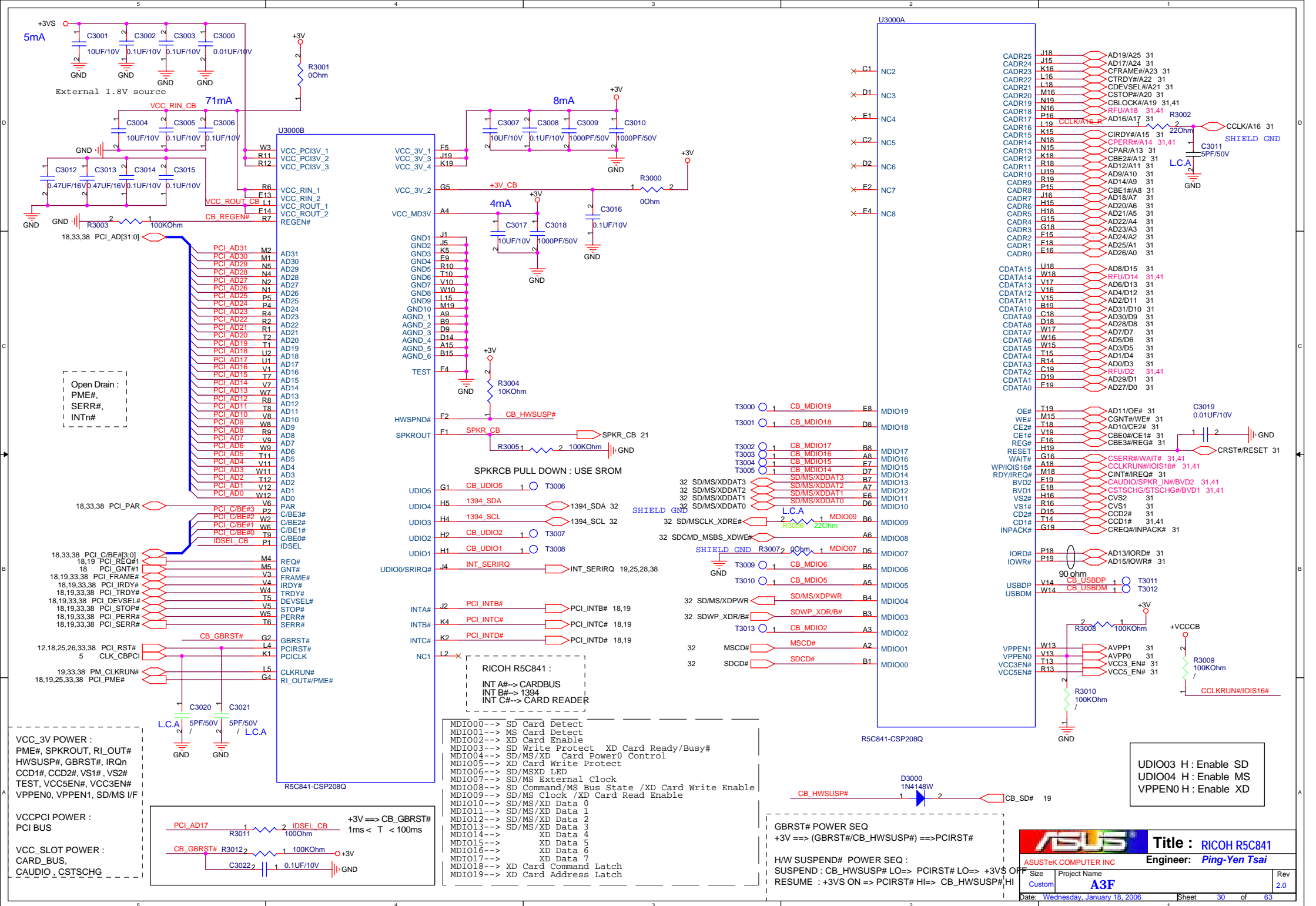
Size  
A4

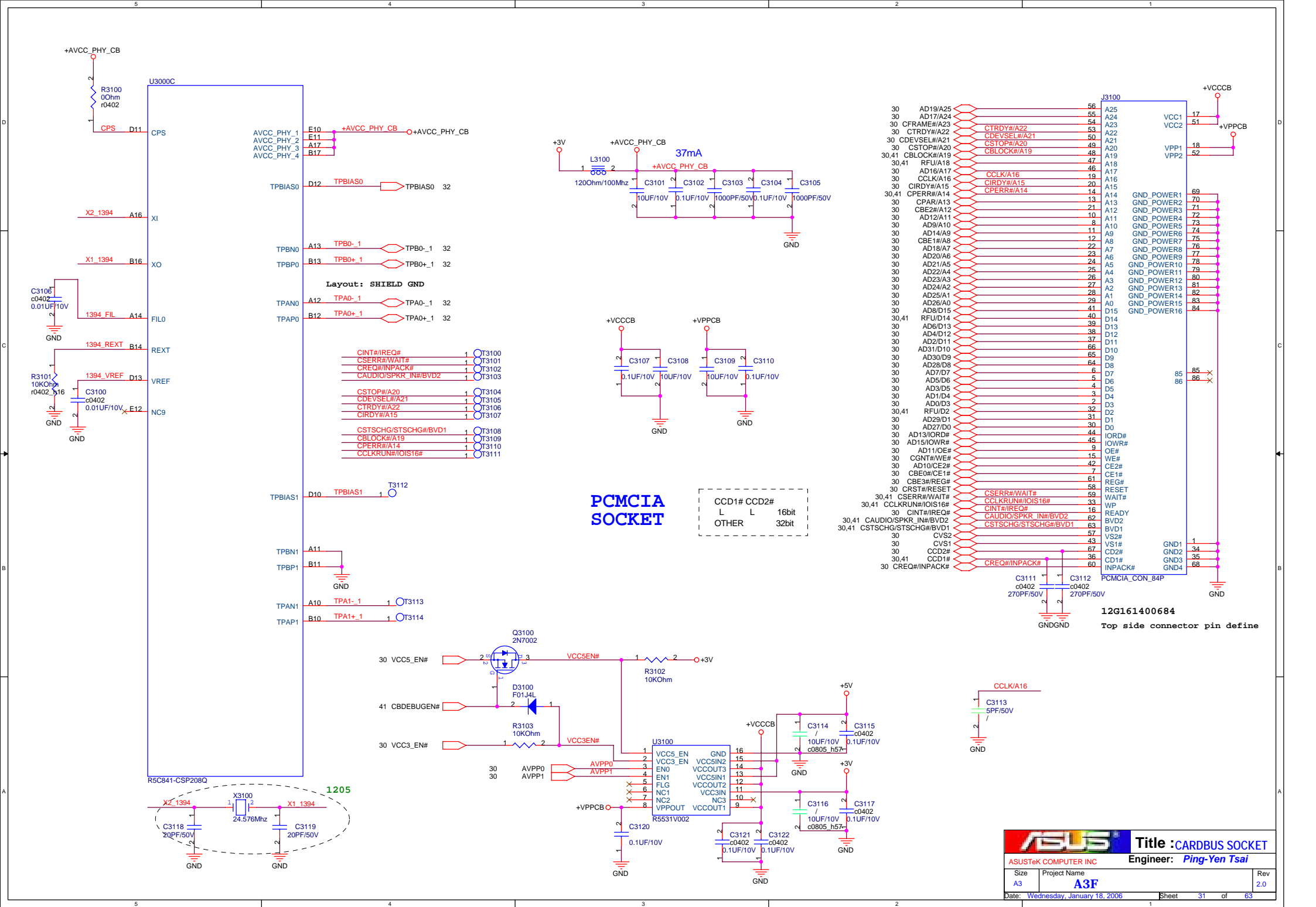
Project Name  
**A3F**

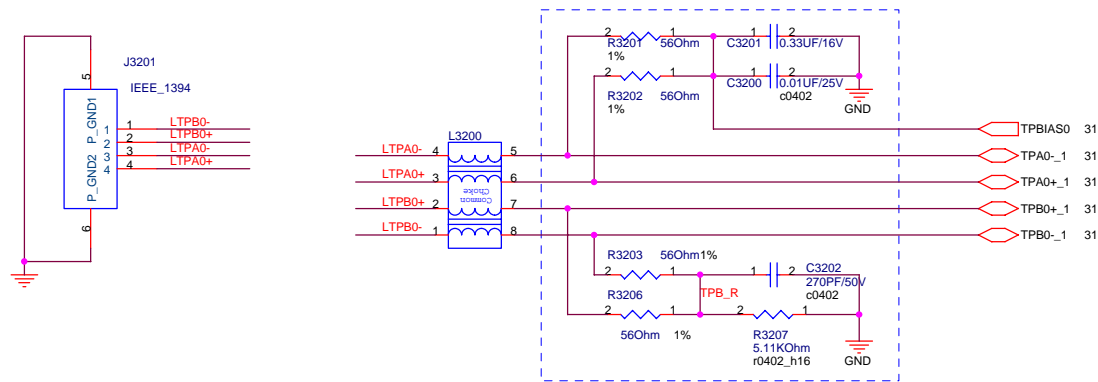
Rev  
2.0

Date: Wednesday, January 18, 2006

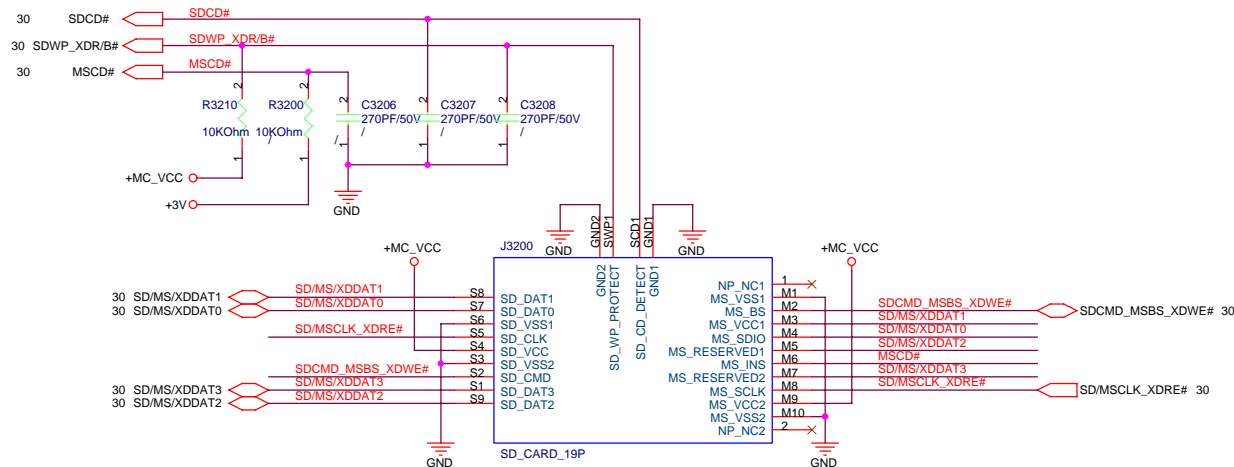
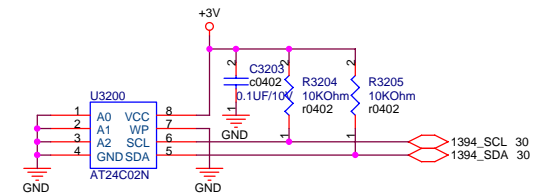
Sheet 29 of 63



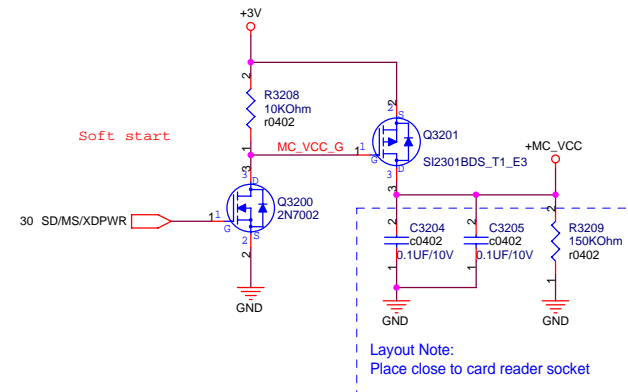




1. Close to R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

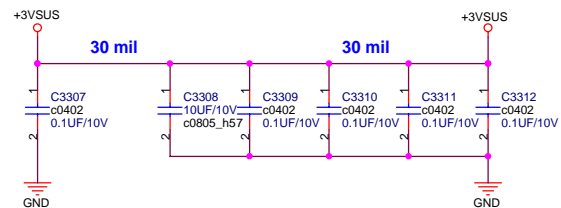


Layout: SHIELD GND

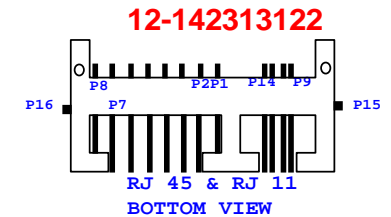
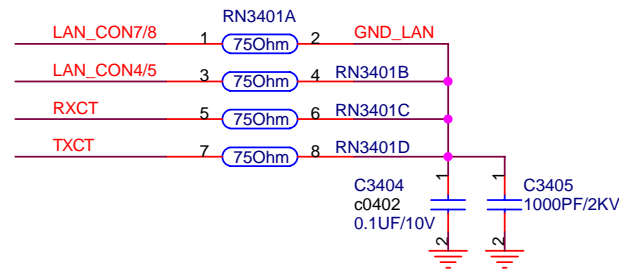
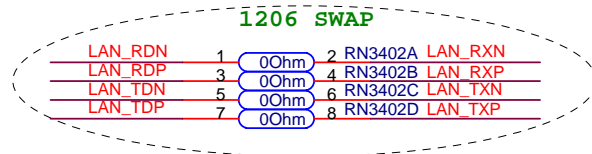
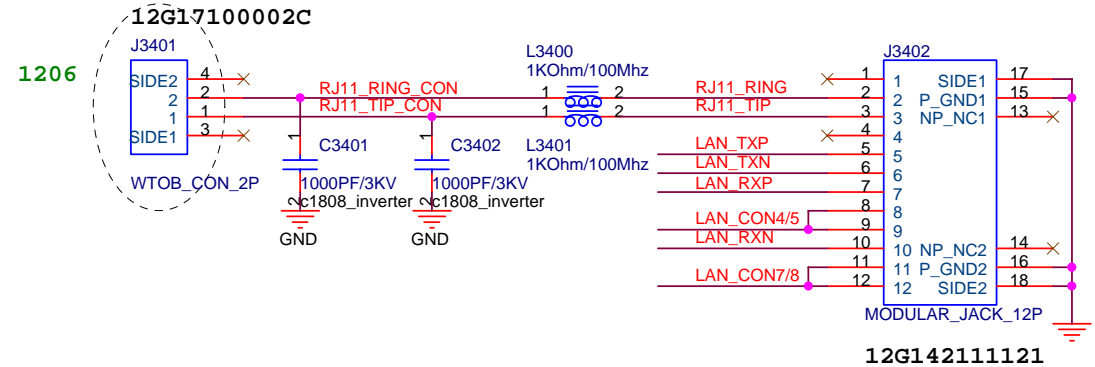
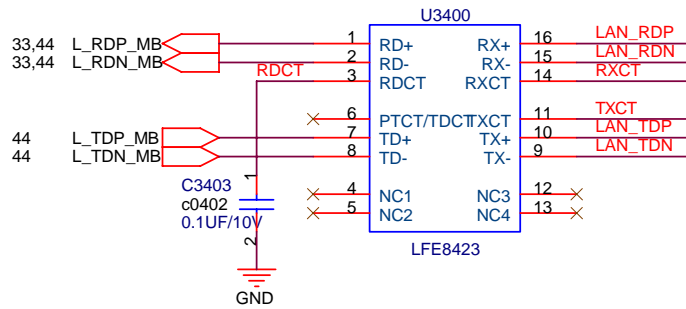


Layout Note:  
Place close to card reader socket

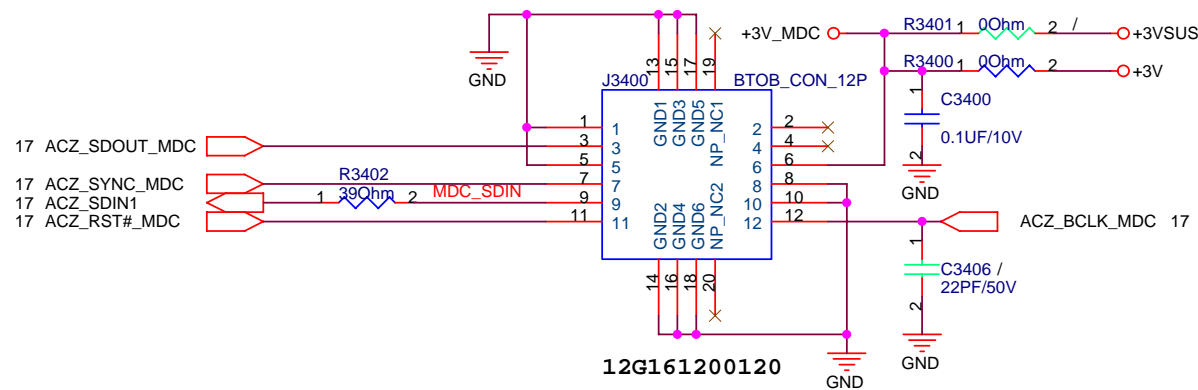




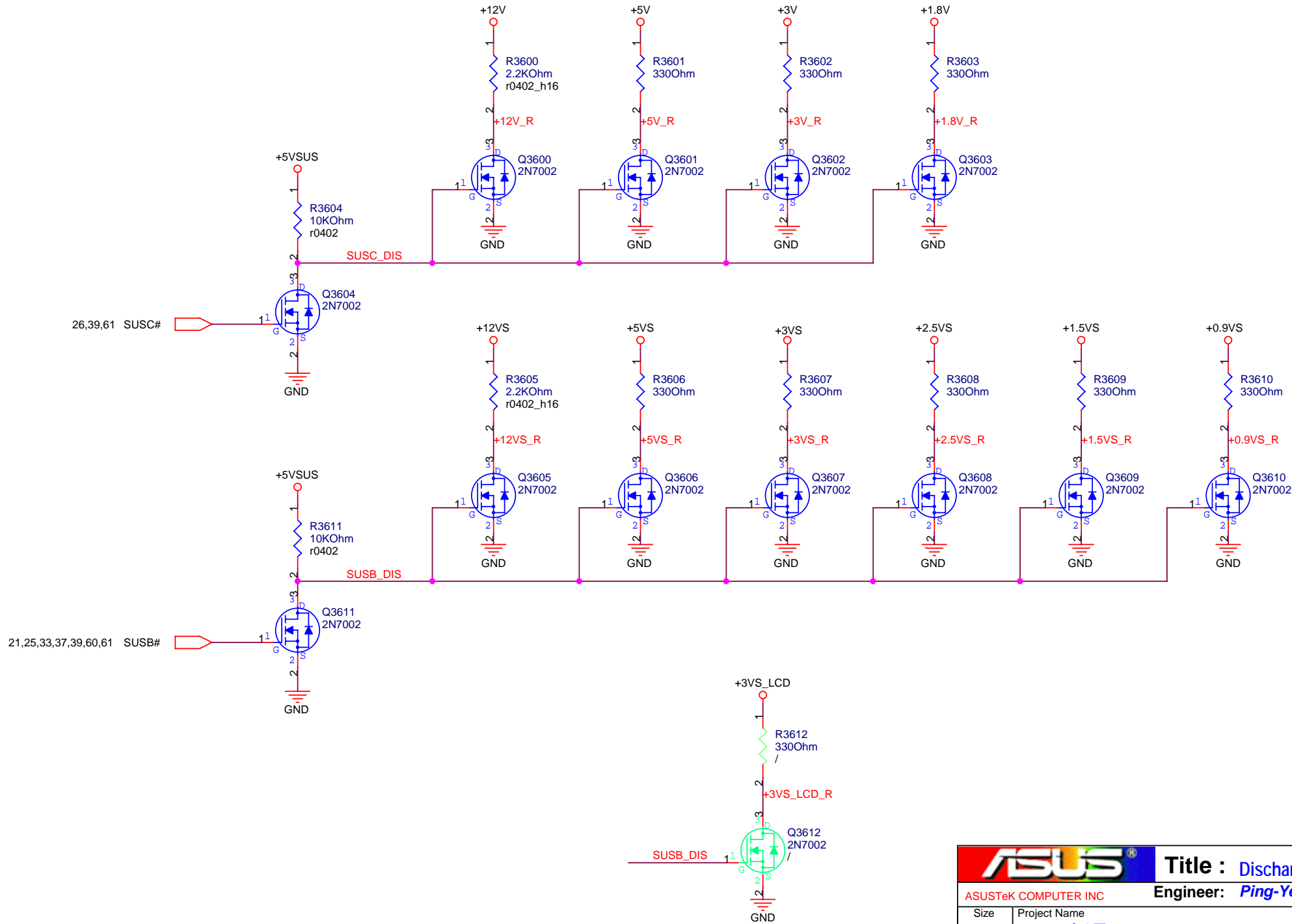
# LAN PORT

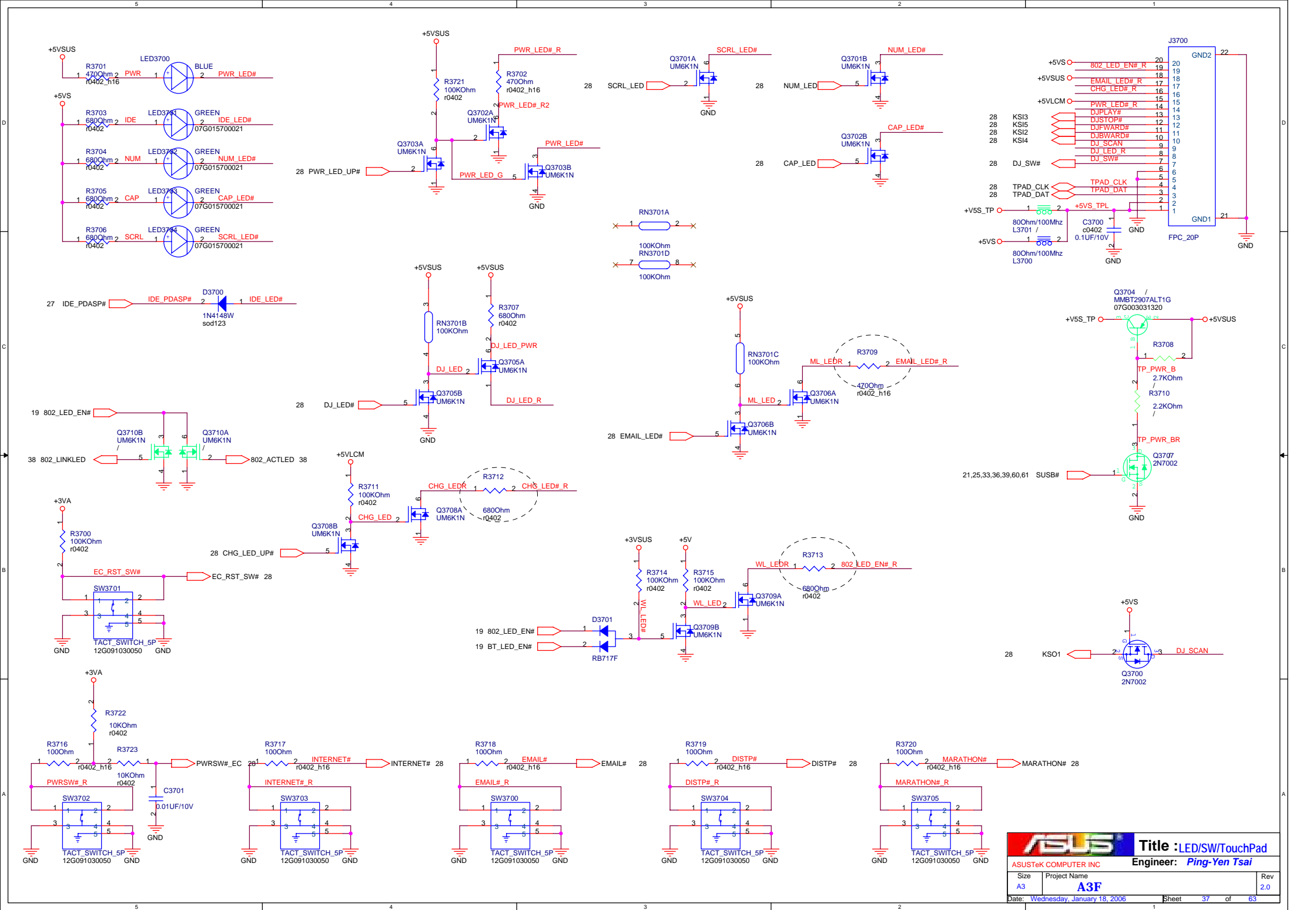


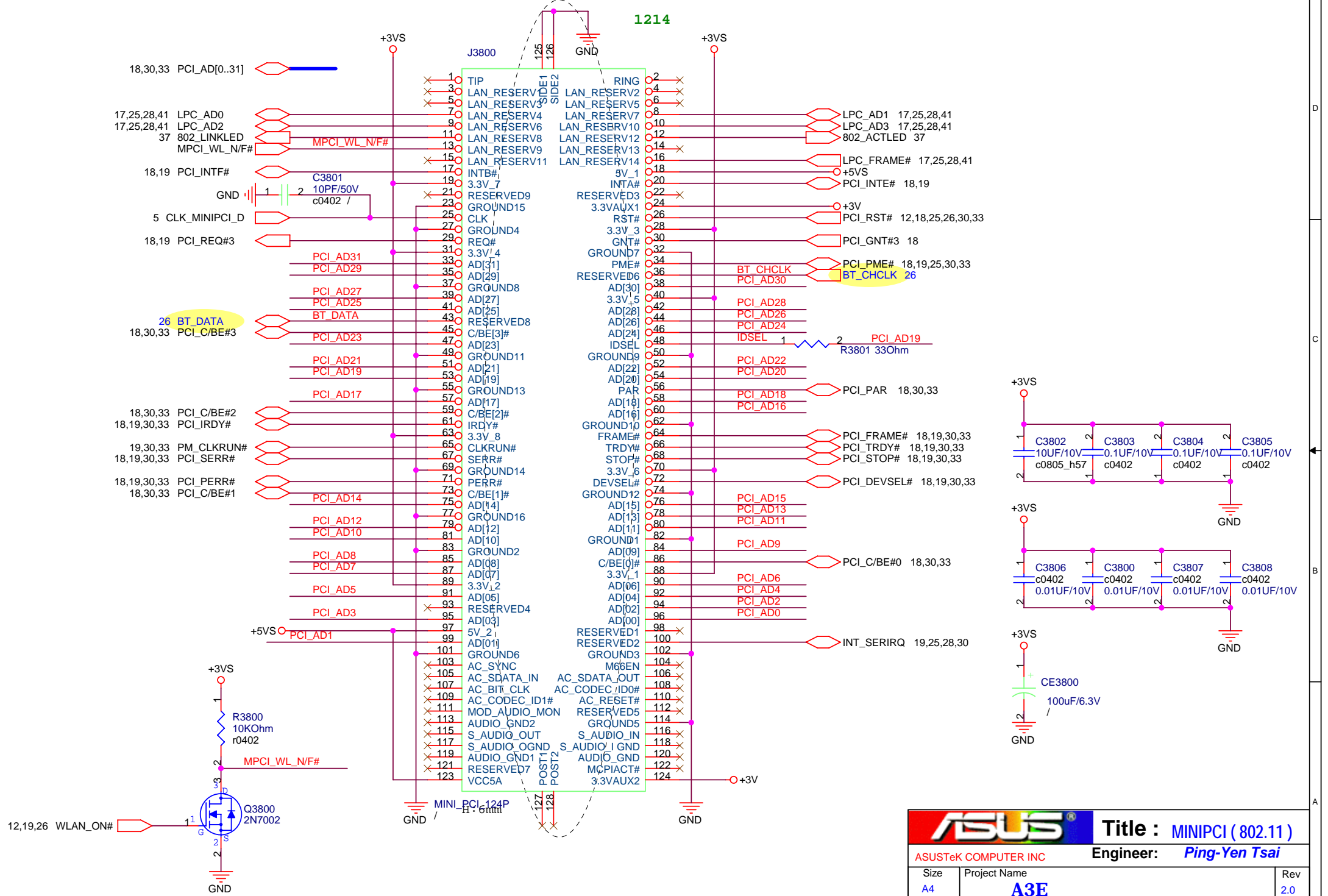
# MDC Conn



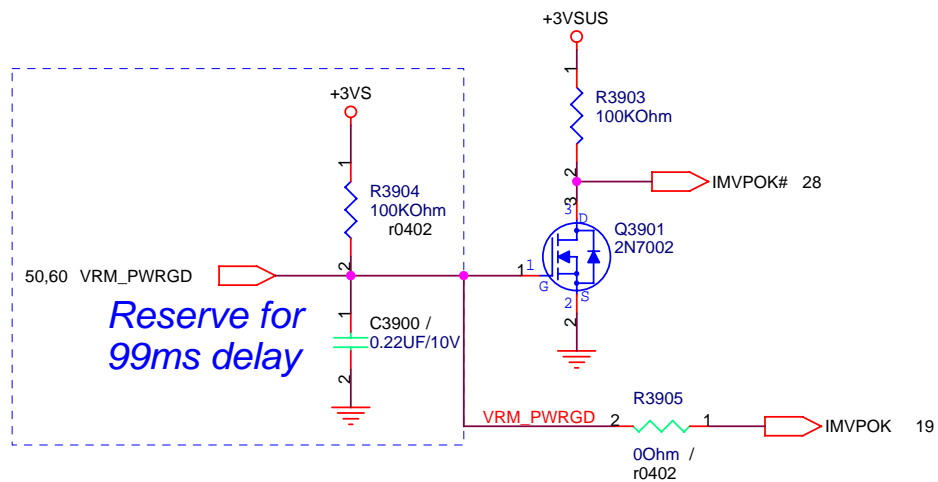
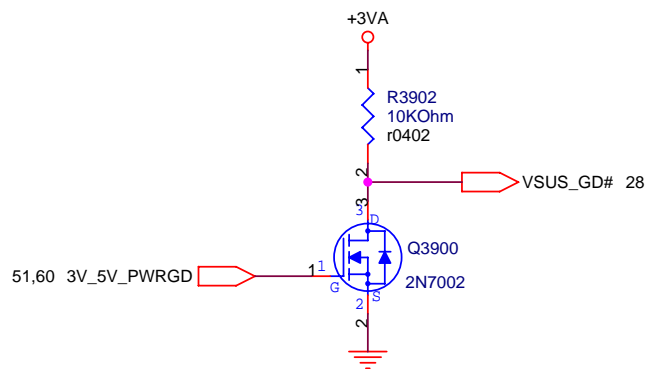
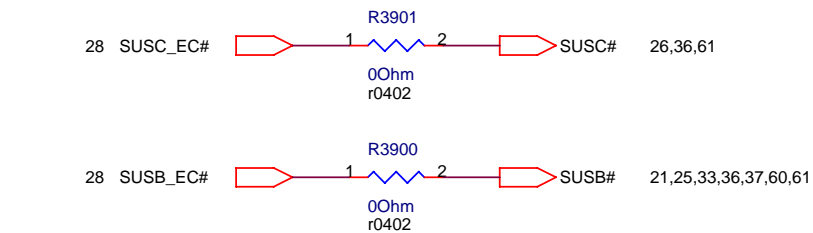




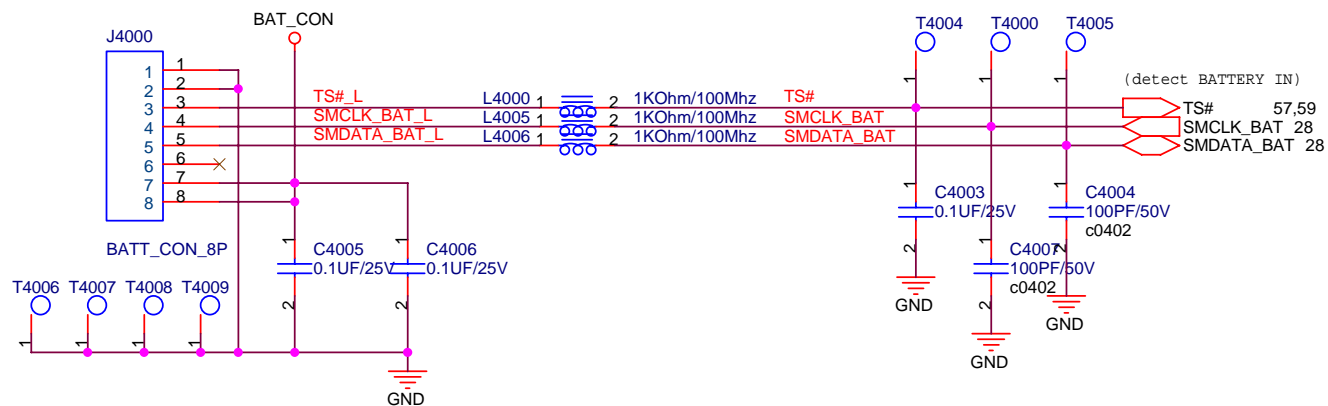
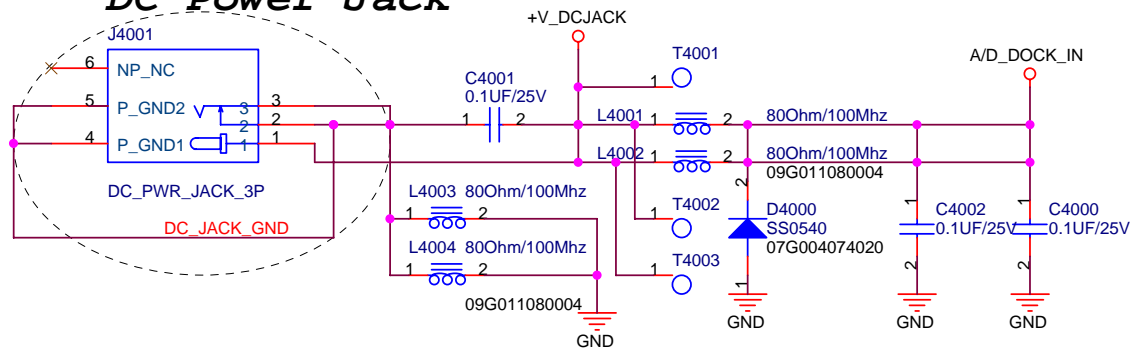






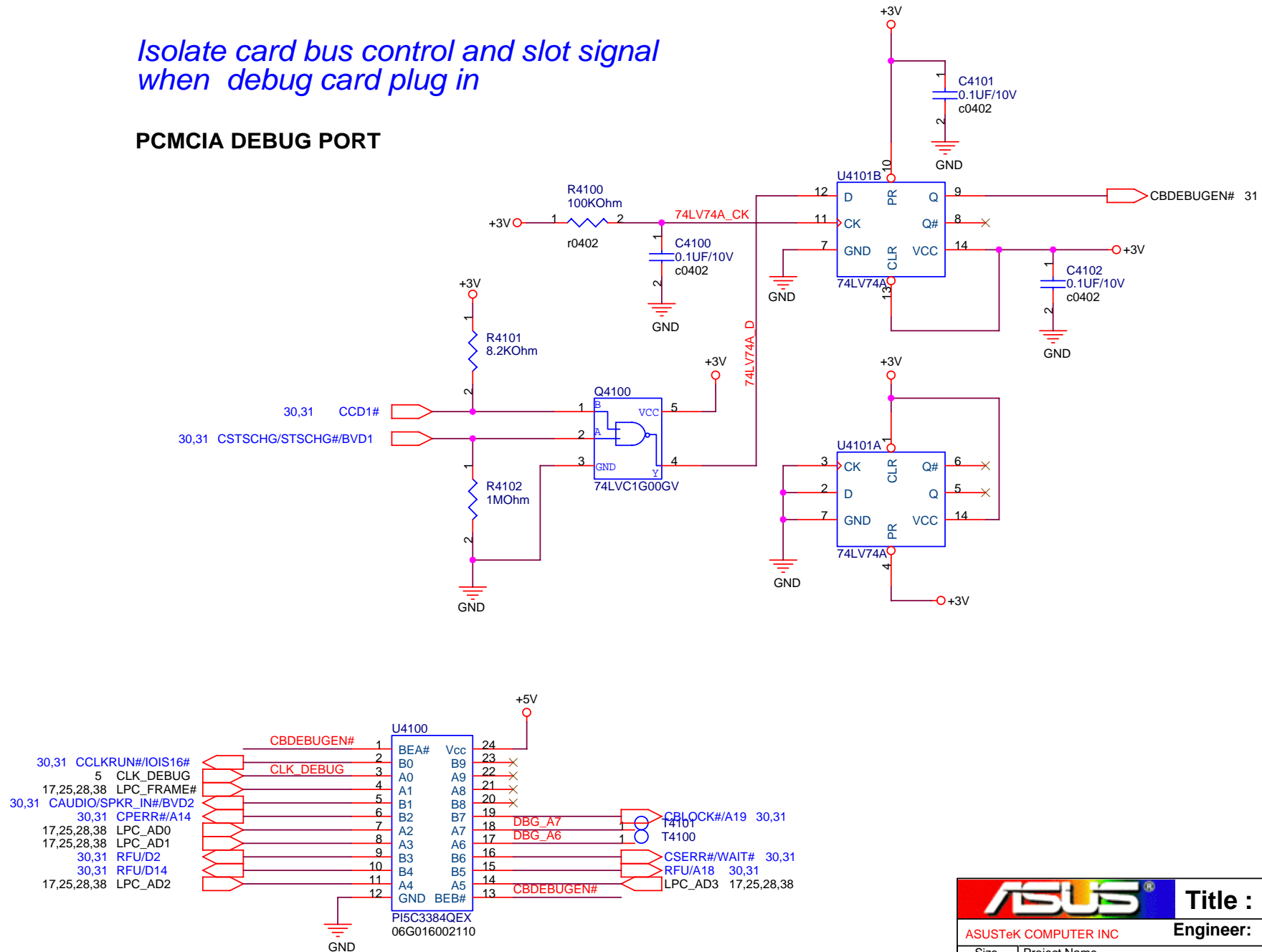


## DC Power Jack

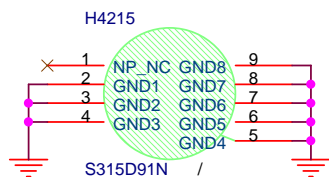
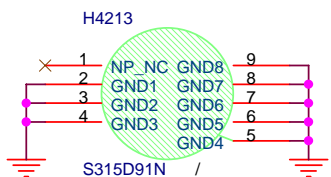
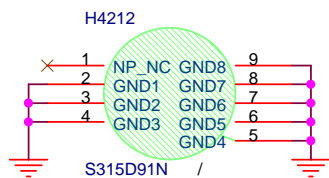
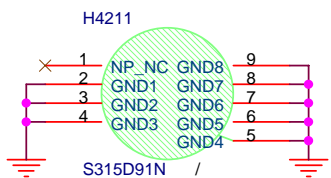
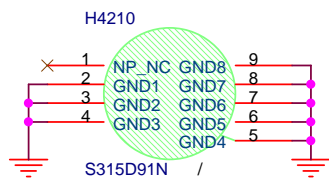
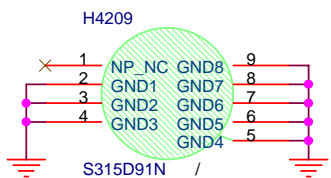
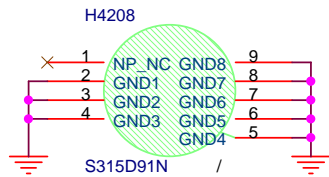
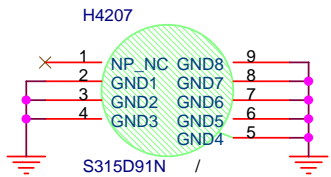
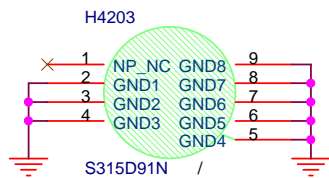
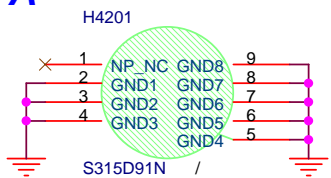


*Isolate card bus control and slot signal  
when debug card plug in*

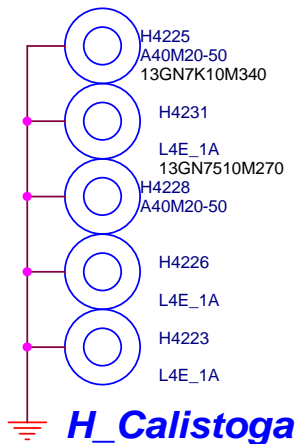
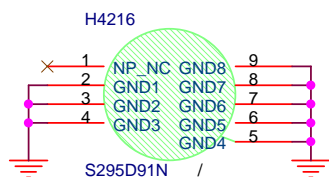
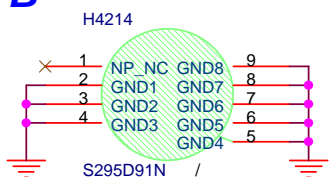
## PCMCIA DEBUG PORT



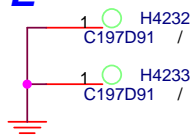
A



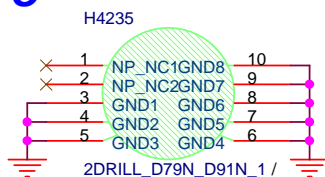
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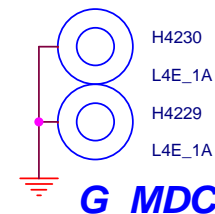
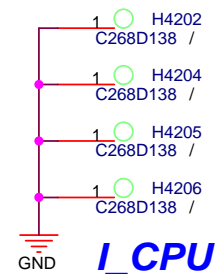
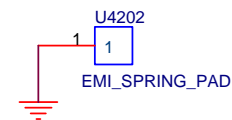
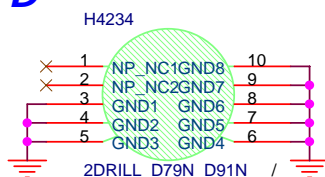
E



C



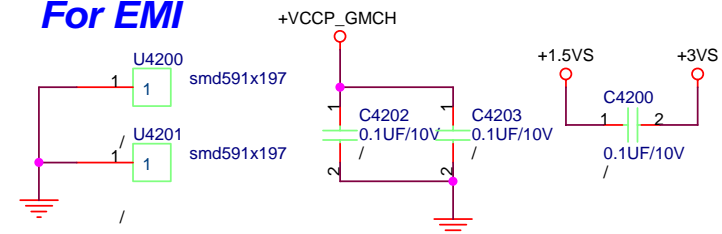
D



J



For EMI



<b>ASUS</b>		<b>Title : SCREW HOLE</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Ping-Yen Tsai</b>	
Size A4	Project Name <b>A3F</b>		Rev 2.0
Date: <b>Wednesday, January 18, 2006</b>		Sheet <b>42</b> of <b>63</b>	


## R1.1

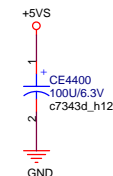
- 11/14 1. Change resistor number from R1 to R1401  
2. Change R1704 value from 10K to 330K  
3. Add U2202 C D E F  
4. Change C2511 value from 0.1uF to 0.047uF(11G232147316360)  
5. Change C2510, C2514 and C2515 value from 0.1uF to 0.33uF(11G232333436030)
- 11/29 1. Remove R409  
2. USB port (J3500) power control on shutdown of AC mode  
3. Change U2202 power source form "+3VS" to "+3V" to solve pop noise  
4. Add D2202 1N 4148W P/N 07G001001612 to solve pop noise when power off  
5. Remove R2201 and mount R2203 to change Gain Setting
- 12/1 1. Change component D2103 DAP202K to 1N4148W P/N 07G001001612  
2. Add Components 10K Ohm & 1N4148W P/N 07G001001612 and connect U2100 pin 30  
3. Change J1500,U900,U2502,U3400,H4225,H4226,H4228,H4229,H4230,H4223,H4231,Q4400 to green part
- 12/2 1. Change Thermal Sensor to SO-8 MAX6657  
2. USB4-->Camera, USB6-->PB
- 12/5 1.Change material CE1200, F3500, F3501, F3502  
2. Add EC new function-->THRO\_CPU  
3. Change X3100, C3118, C3119 J3401 part number
- 12/7 1.Change J2500 footprint
- 12/9 1.Change R1202 value

## R2.0

- 1/2 1. BOM Add R1943, Remove R1919  
2. BOM Add D2105, R2125  
3. BOM Add C2223  
4. BOM Add R3505, Q3505, U3500  
5. Schematics Add R3503, R3504 but don't mount  
6. Schematics Add R4418~R4424 but don't mount
- 1/4 1. change R3709, R3712 & R3713 value
- 1/6 1. Add Power schematics & GPIO35 (Add R1944,R1945)

- 1/9 1. Remove JP3500, Add R3506, R3507
- 1/10 1. Add R415, BOM remove R408 Q403
- 1/11 1. Change C404 to 0.47uF  
2. Change DJ JACK part number

		Title : HISTORY	
ASUSTeK COMPUTER INC		Engineer: Ping-Yen Tsai	
Size Custom	Project Name A3F		Rev 2.0
Date: Wednesday, January 18, 2006		Sheet	43 of 63



OE	S	Out
L	L	I0
L	H	I1
H	X	NC



OE#	IN	Out
L	L	S1
L	H	S2
H	X	Disable





1

1

8

**A**

5

4

3

2

1

1

1

8

**A**

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5

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4

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3

2

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Title
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<Title>

Size  
A

Document Number  
A3F

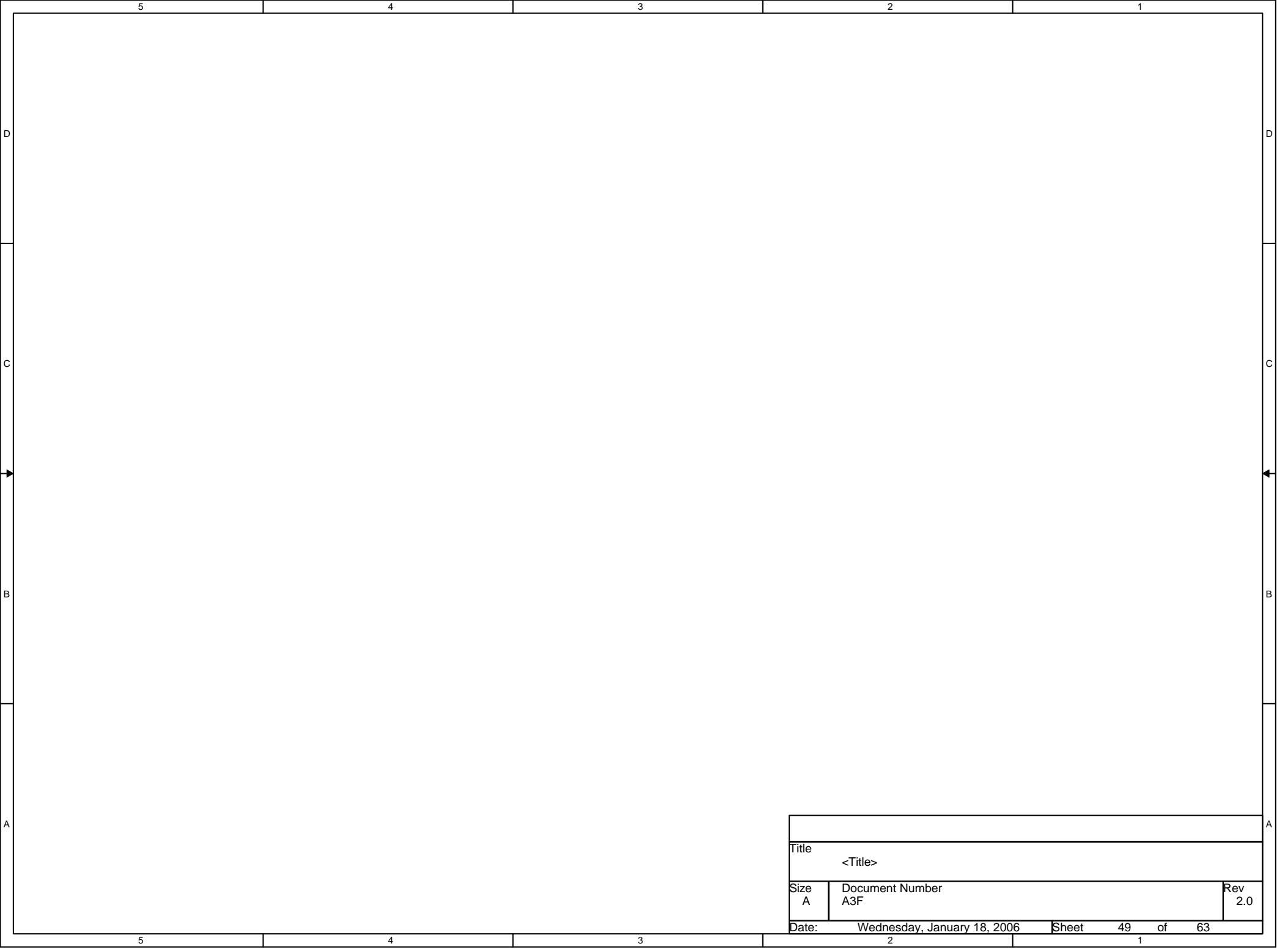
Rev	2.0
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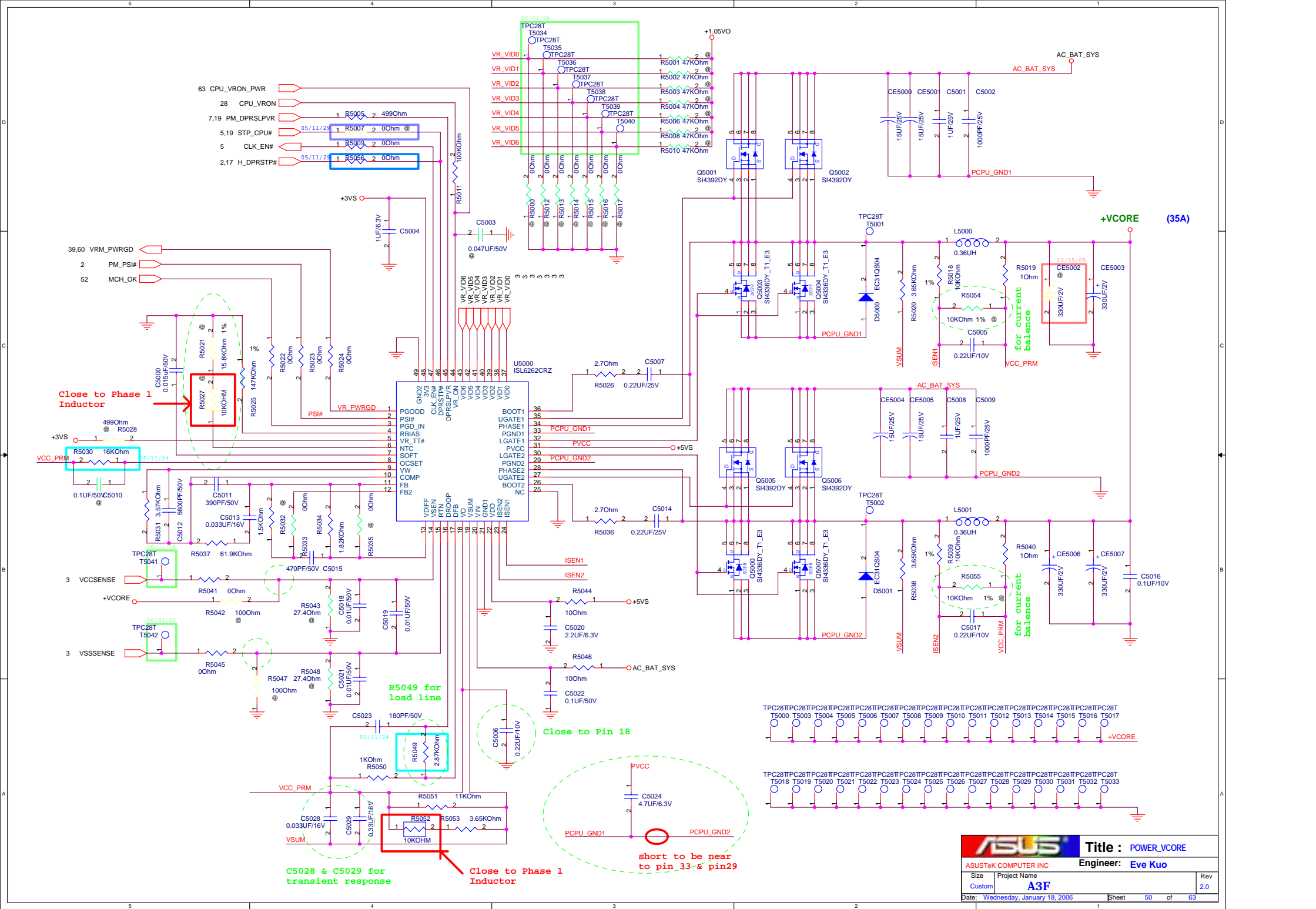
Date: Wednesday, January 18, 2006 Sheet 45 of 63





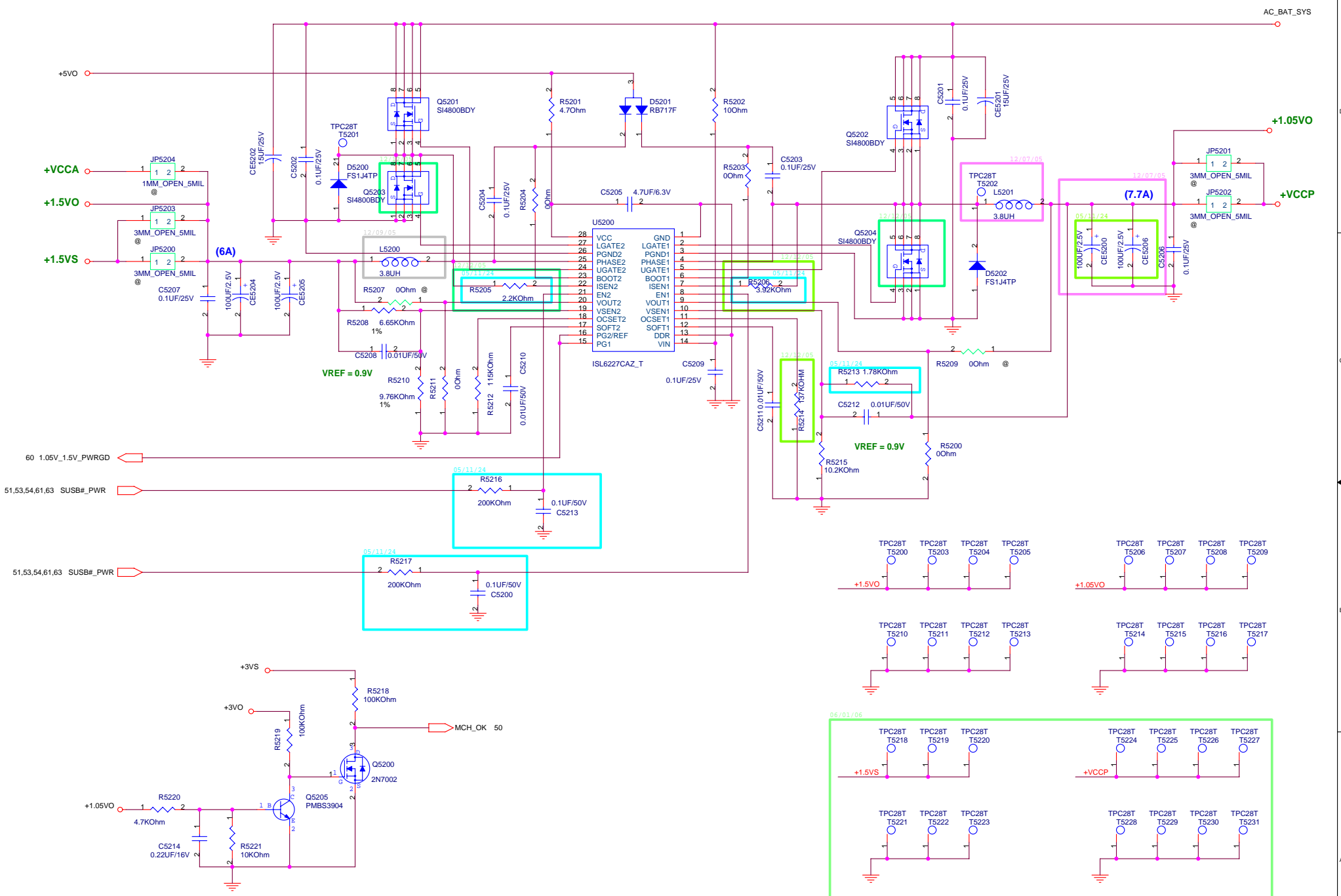


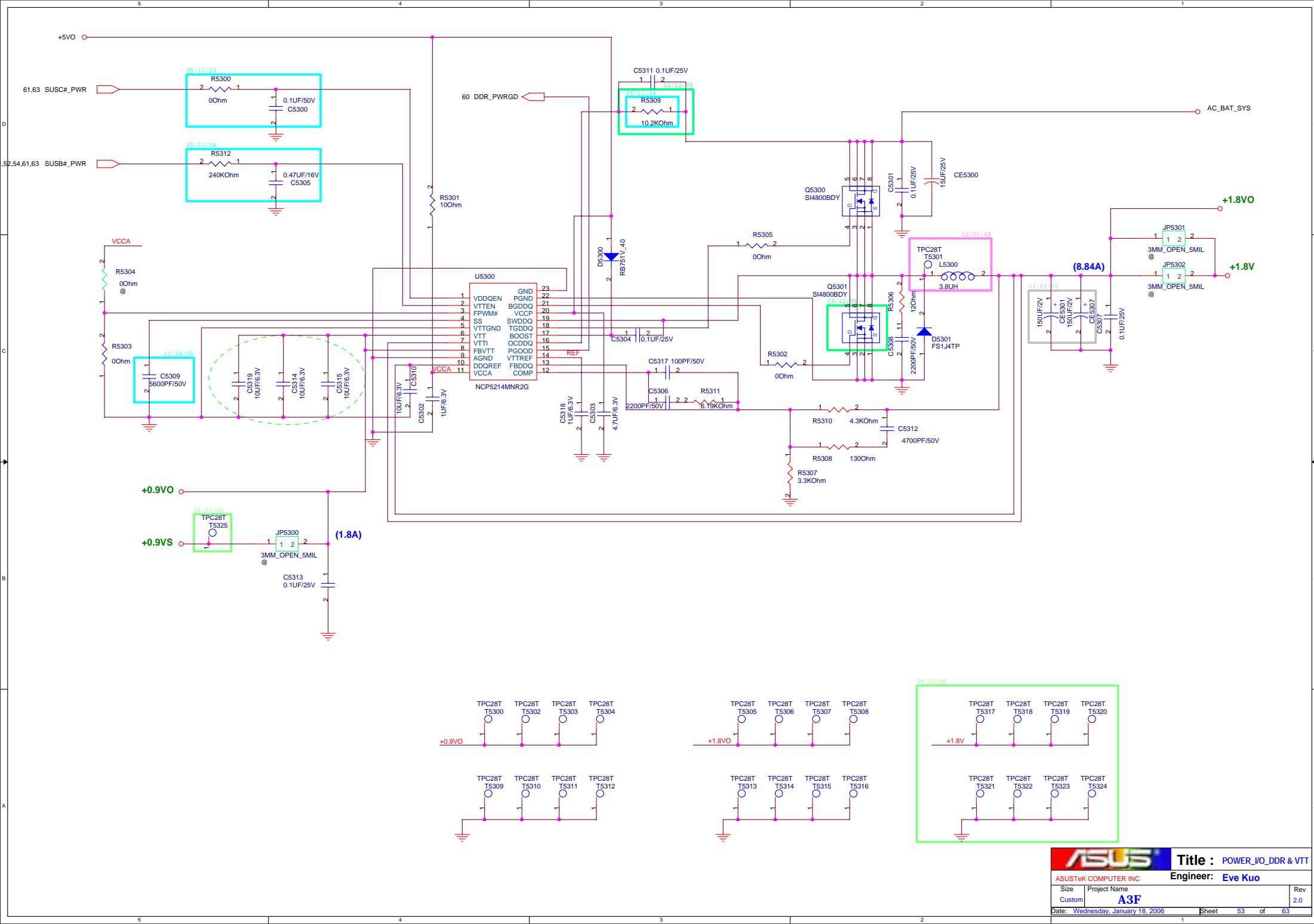




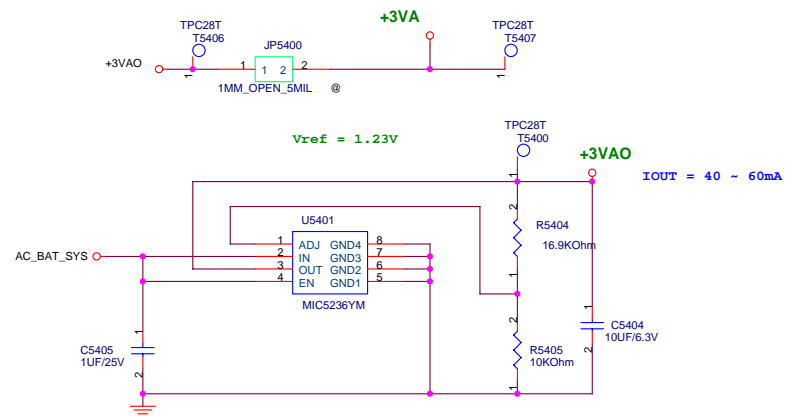




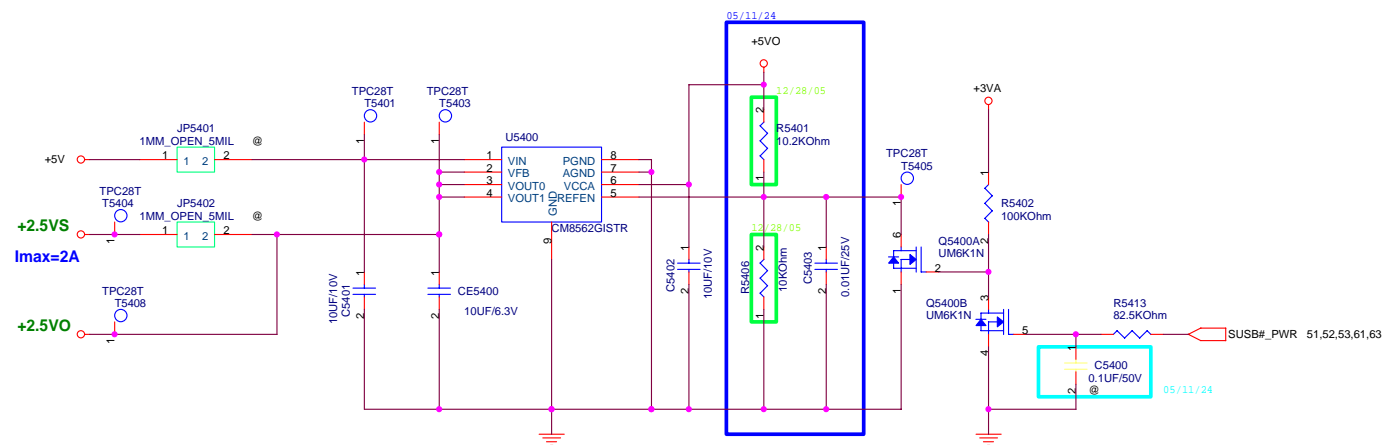




+3VAO



+2.5Vs



R1.0

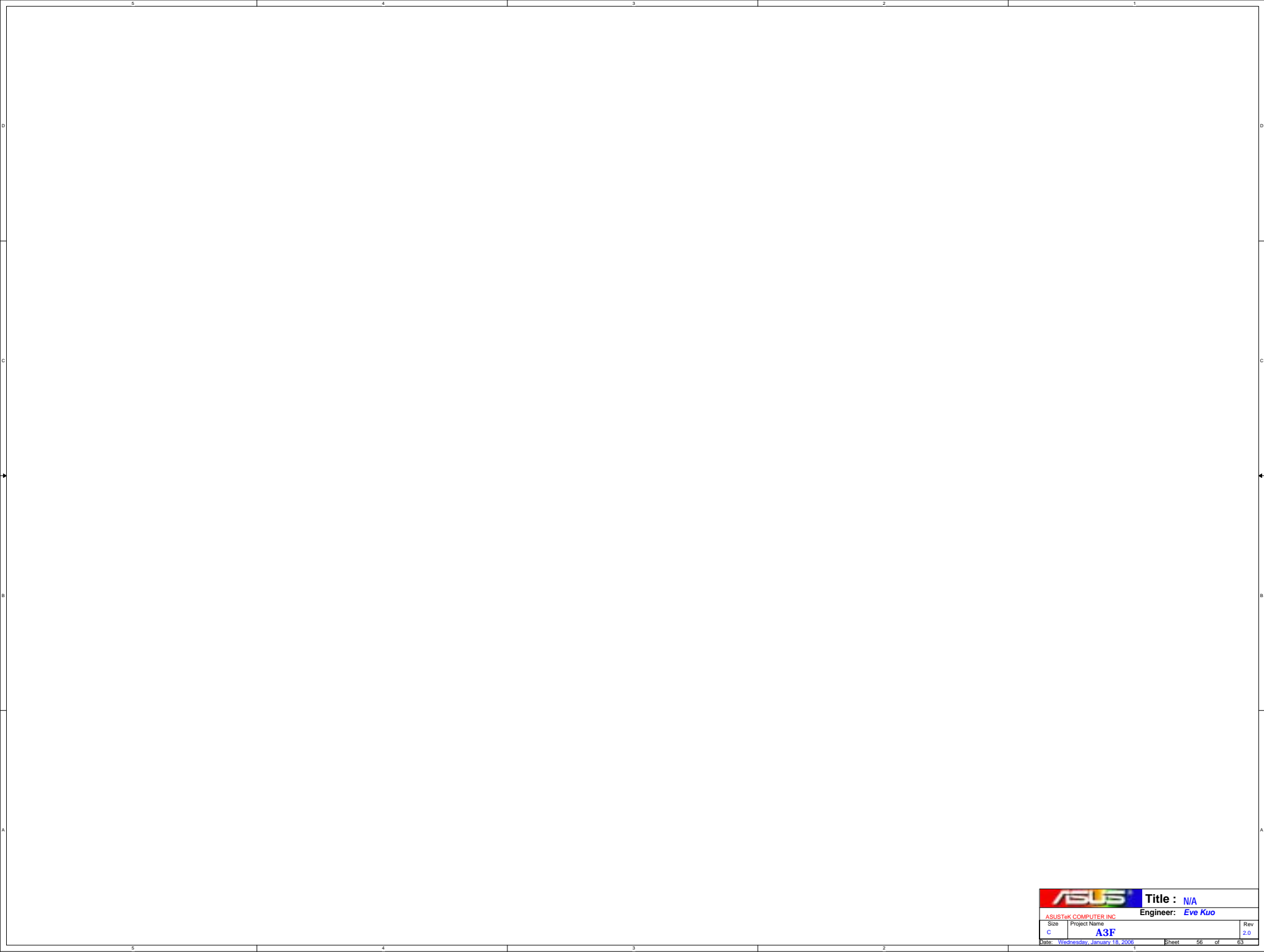
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R1.1

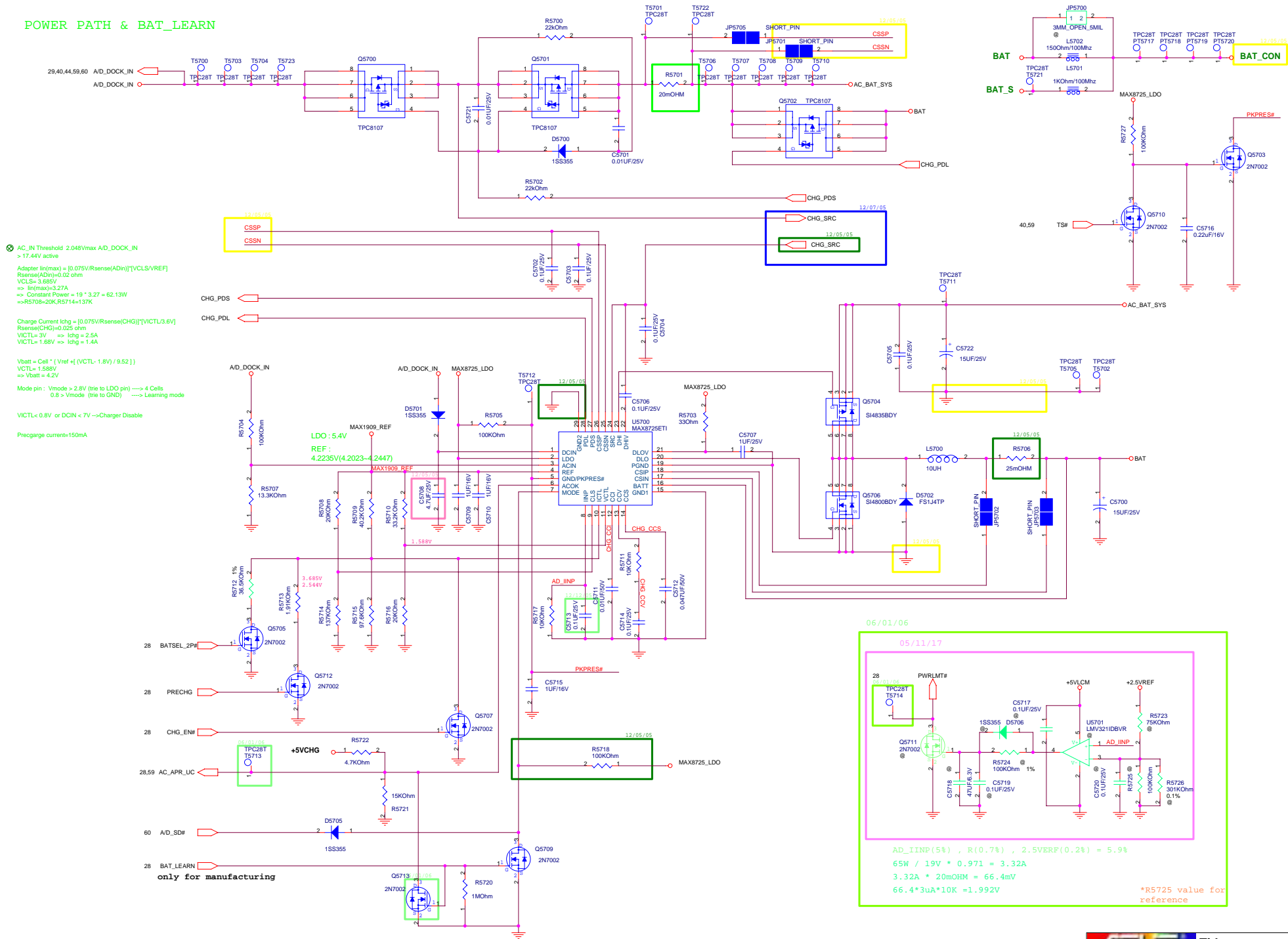
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R2.0

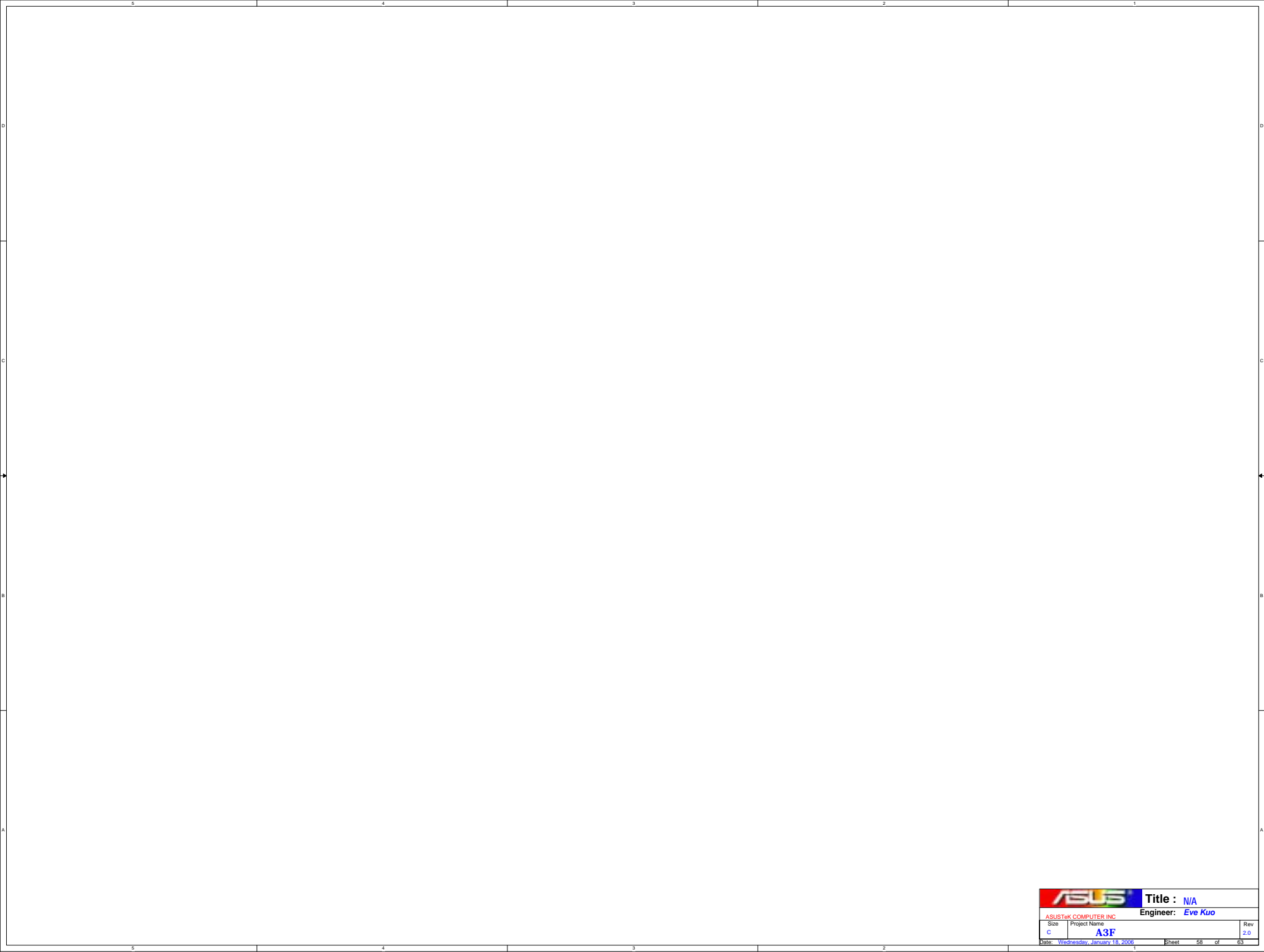
Item	Before	After	Reason	Owner	Date



## POWER PATH & BAT\_LEARN







9



## 3 |

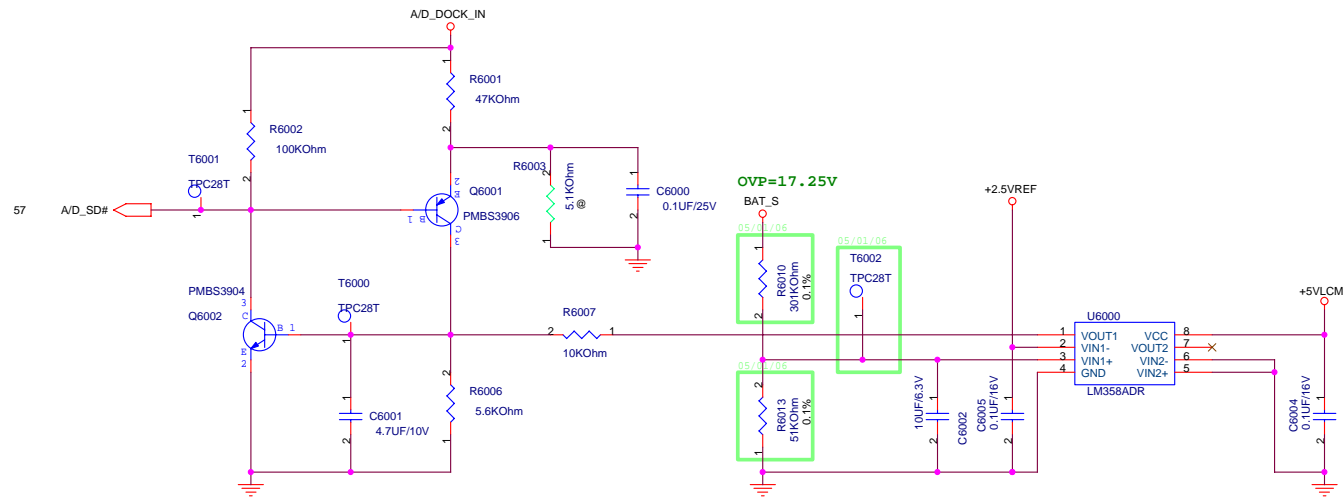
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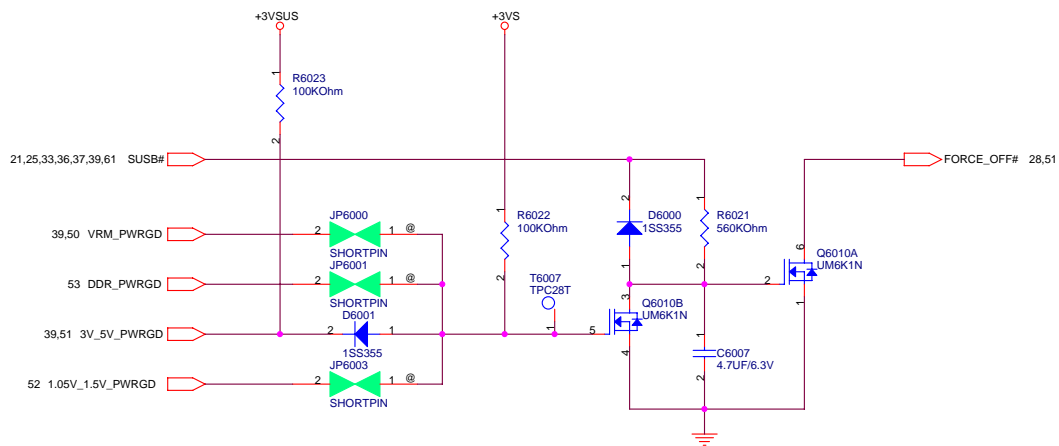
L



## BATTERY A/D\_SD# (OVP)

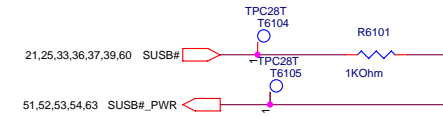
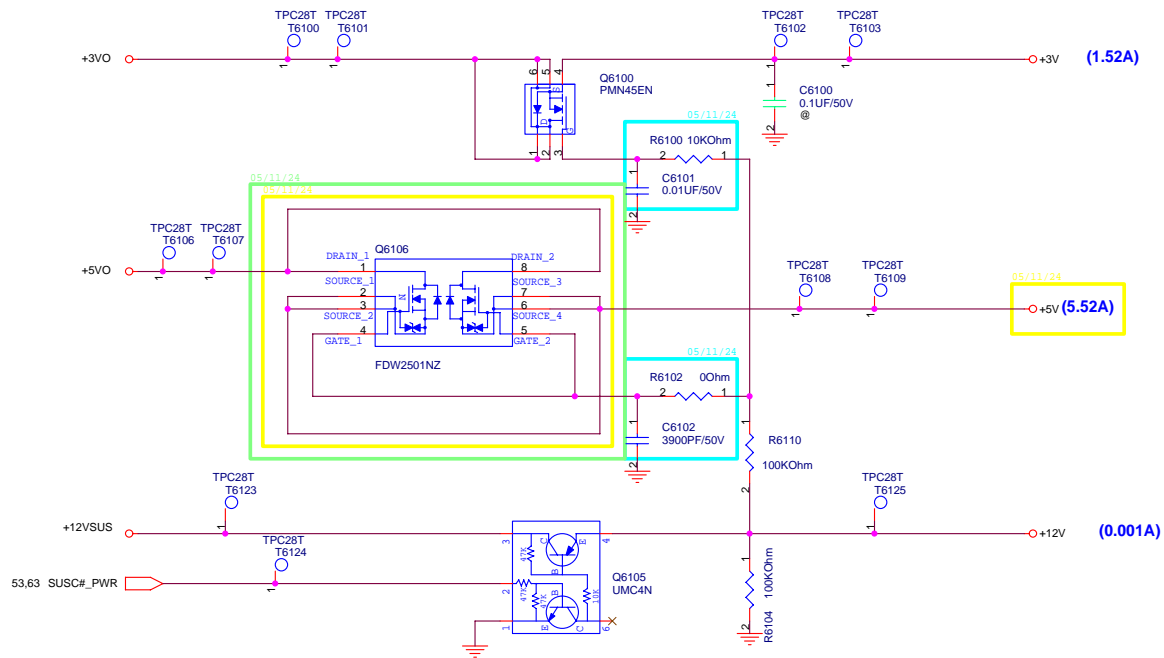


## POWER GOOD DETECTER

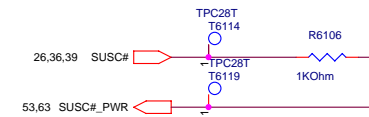
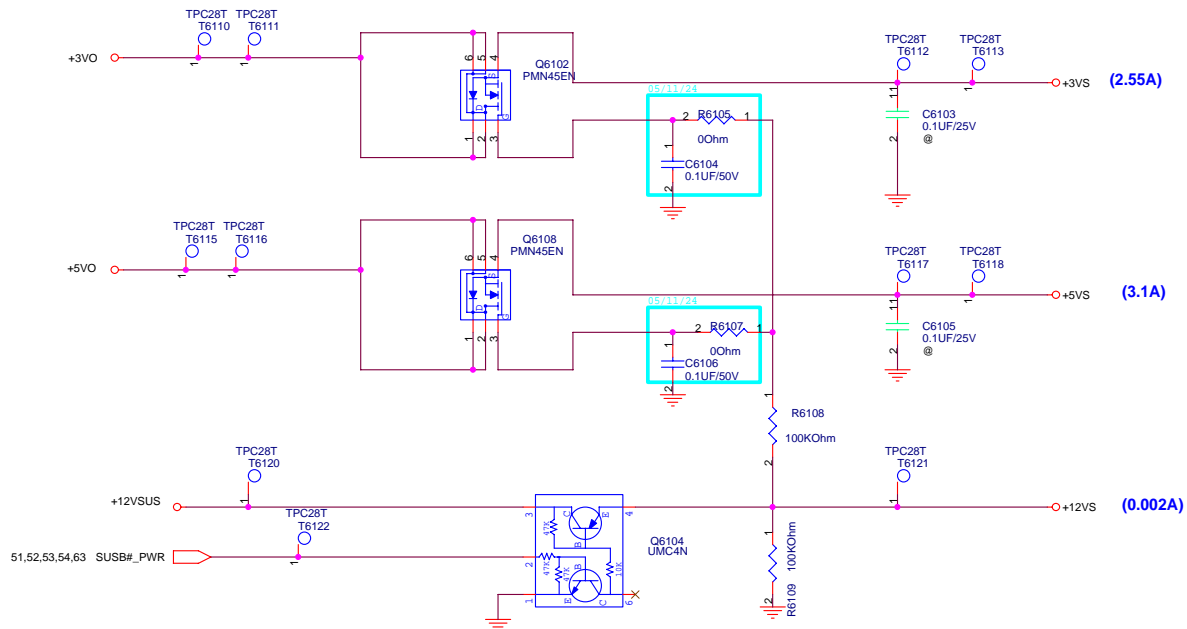


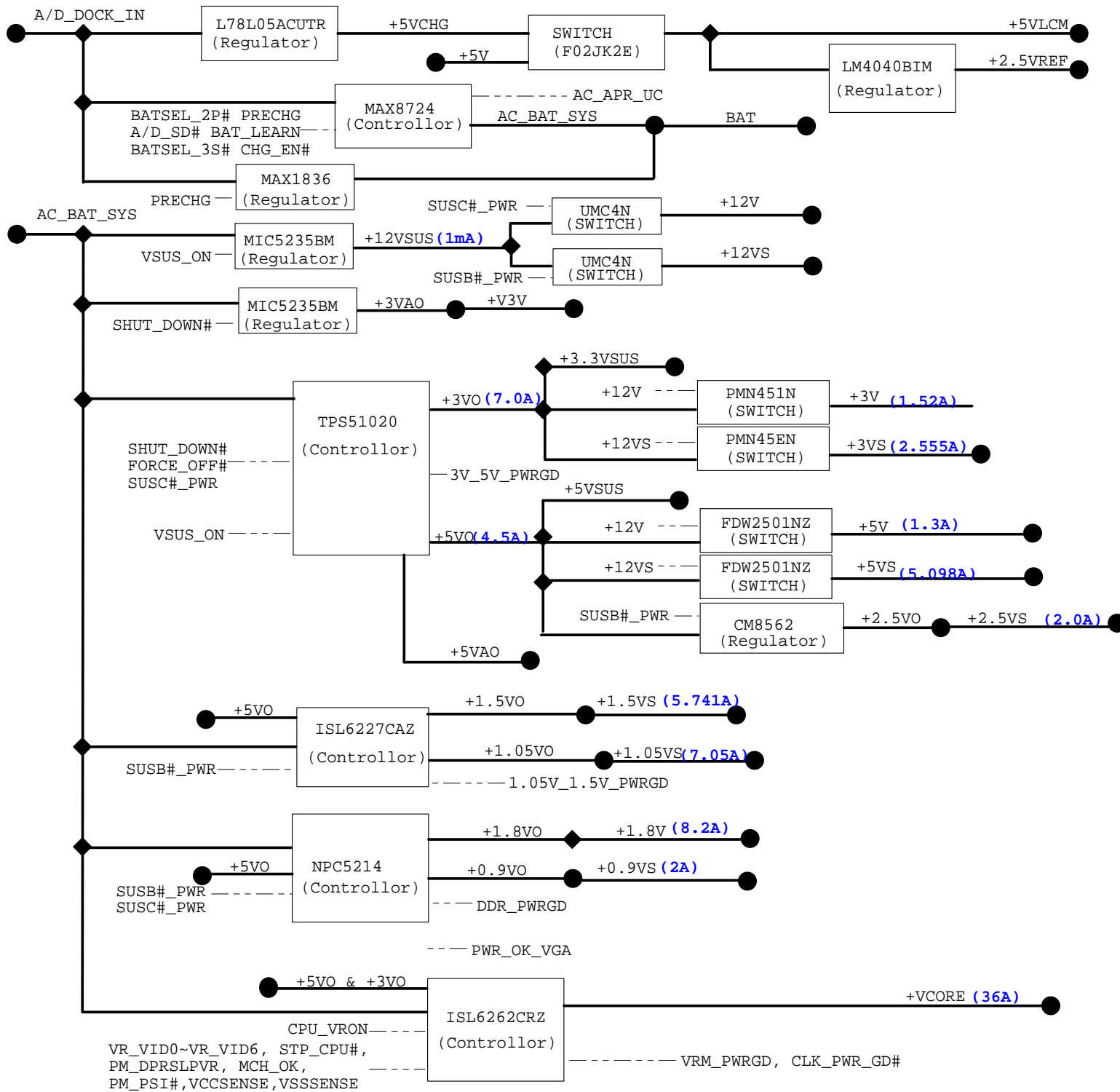
TPC28T	T6003	VRM_PWRGD
TPC28T	T6004	DDR_PWRGD
TPC28T	T6005	3V_5V_PWRGD
TPC28T	T6006	1.05V_1.5V_PWRGD

## SUSC#\_PWR POWER



## SUSB#\_PWR POWER







FOR POWER TEST

